CiteSeer Find: mpp and serial and (single or one | Documents | Citations

Searching for **mpp and serial and (single or one or 1) bit**.
Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
6 documents found. **Order: citations weighted by year.**

Performance Analysis of Four SIMD Machines - Rod Fatoohi (1993) (Correct) (5 citations)
machines are: a 32k processor CM2, a 16k processor **MPP**, a 16k processor MasPar MP-1, and a 4k processor
NN: Nearest Neighbor The CM2 at NAS has 32k **1-bit serial** processors and 1024 processing elements (PEs)
the programming language used. The performance of **Single** Instruction Multiple Data (SIMD) machines has
ftp.ai.mit.edu/pub/users/misha/backup/vision/RNR-92-034.ps.gz

One or more of the query terms is very common - only partial results have been returned. Try Google (RI).

Performance Instrumentation Techniques for Parallel Systems - Reed (1993) (Correct) (4 citations)
Machines CM-5, Ncube/3, Cray T3D, and Convex **MPP**. System Software Hardware Run-time System
MIMD. Exemplars of these classes include the **bit-serial** SIMD Thinking Machines CM-2, the shared memory
the variance in performance is high, both in a **single** application and across a group of applications)
vibes.cs.uiuc.edu/Publications/Papers/Springer.ps.gz

Processing Element and Custom Chip Architecture for the.. - Revision Donald (1987) (Correct) (1 citation)
systems are the Massively Parallel Processor (**MPP**) built by Goodyear Aerospace Corporation (now
of an individual PE. They operate in **bit-serial** fashion. VLSI technology is essential to the
speedup is the use of many processors driven by a **single** control unit. This is the **single** instruction
www.cse.ucsc.edu/~rph/ce290ms96/blitz_tr.ps

The Disputer : A Dual Paradigm Parallel Processor for Graphics.. - Ian Page (Correct)
such as the DAP (Reddaway, 1973)CLIP (Duff, 1976)**MPP** (Batcher, 1980)and the Connection Machine
Vision. The seed that germinated into today's **bit-serial**, SIMD processor arrays was a paper by Shooman
of pixels. For this type of algorithm, the SIMD (**Single** Instruction Stream, Multiple Data Stream, or
ftp.comlab.ox.ac.uk/pub/Documents/techpapers/Ian.Page/disputer.ps.gz

The Interlocking Bus Network For Fault-Tolerant Processor.. - Siegle, Reeves, Kozminski (Correct)
are Illiac-IV[1]the Connection Machine[2]the **MPP**[3]and BLITZEN[4]The processors are connected
and has a word width of **1 bit**, i.e. it is **bit-serial**. In the full-scale version, 128 chips are
The processors normally operate in SIMD mode (**single** instruction stream, multiple data stream)in
faui79.informatik.uni-erlangen.de/pub/doc/interlock.ps.Z

A data parallel implementation of the TRFD program from the.. - David Lilja (1994) (Correct)
www.cs.umn.edu/Research/Agassiz/agassiz
used in these experiments consists of p=32768 **bit-serial** processors running at 10 MHz. **One** 32-**bit**
these types of machines to the massively parallel **single**-instruction stream, multiple-data stream (SIMD)
ftp-mount.ee.umn.edu/pub/faculty/lilja/papers/trfd.mpp.ps.Z

Try your query at: Amazon Barnes & Noble Google (RI) Google (Web) CSB DBLP

CiteSeer - citeseer.org - Terms of Service - Privacy Policy - Copyright © 1997-2002 NEC Research Institute

PORTAL LIBRARY

> home > about > feedback > logout

US Patent & Trademark Office

Search Results

Search Results for: [mpp and (single bit or one bit or 1-bit) and bit serial]
Found 14 of 98,251 searched. -> Rerun within the Portal

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: **Title** **Publication** **Publication Date** **Score** Binder

Results 1 - 14 of 14 **short listing**

1 GPFP: an array processing element for the next generation of massively parallel supercomputer architectures 82%
Don Beal , Costas Lambrinoudakis
Proceedings of the 1991 conference on Supercomputing August 1991

2 A fault tolerant, bit-parallel, cellular array processor 80%
Steven G. Morton
Proceedings of 1986 fall joint computer conference on Fall joint computer conference November 1999

3 Message-passing algorithms for a SIMD torus with coteries 77%
M. Herbordt , C. Weems , J. Corbett
Proceedings of the second annual ACM symposium on Parallel algorithms and architectures May 1990

4 Programming environments for highly parallel multiprocessors 77%
A. P. Reeves
Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1 January 1988
Emerging highly parallel multiprocessors offer an exciting alternative to conventional pipelined supercomputers for a variety of computationally intensive scientific applications. A factor that

has impeded the introduction of these multiprocessor systems is that conventional languages, such as Fortran, cannot be directly used and new programming techniques must be mastered. A key issue for highly parallel systems is the development of appropriate programming environments. Program ...

5 Compiling Fortran 8x array features for the connection machine computer system 77%

Eugene Albert , Kathleen Knobe , Joan D. Lukas , Guy L. Steele
ACM SIGPLAN Notices , Proceedings of the ACM/SIGPLAN conference on Parallel programming: experience with applications, languages and systems January 1988
Volume 23 Issue 9

The Connection Machine® computer system supports a data parallel programming style, making it a natural target architecture for Fortran 8x array constructs. The Connection Machine Fortran compiler generates VAX code that performs scalar operations and directs the Connection Machine to perform array operations. The Connection Machine virtual processor mechanism supports elemental operations on very large arrays. Most array operators and intrinsic functions map into single instructions or ...

6 A bit-plane architecture for optical computing with two-dimensional symbolic substitution 77%

A. Louri , K. Hwang
The 15th Annual International Symposium on Computer architecture June 1988

A novel architecture based on optical technology is presented for constructing parallel computers. The architecture exploits optics for its ultra-high speed, massive parallelism, and dense connectivity. The processing is based on a new technique called 2-D symbolic substitution which can be implemented with very fast optical components. Two-dimensional symbolic substitution algorithms are developed for arithmetic/logic operations as well as for complex scientific computatio ...

7 Concurrency and parallelism—future of computing 77%

M. Andrews , J. S. Walicki
Proceedings of the 1985 ACM annual conference on The range of computing : mid-80's perspective: mid-80's perspective October 1985

8 Architecture of a massively parallel processor 77%

Kenneth E. Batcher
25 years of the international symposia on Computer architecture

(selected papers) August 1998

9 On the benefit of supporting virtual channels in wormhole routers 77%

Richard J. Cole , Bruce M. Maggs , Ramesh K. Sitaraman
Proceedings of the eighth annual ACM symposium on Parallel algorithms and architectures June 1996

10 S-connect 77%

Andreas G. Nowatzyk , Michael C. Browne , Edmund J. Kelly , Michael Parkin
ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture May 1995 Volume 23 Issue 2

11 Pseudo MIMD array processor—AAP2 77%

T. Kondo , T. Tsuchiya , T. Kitamura , Y. Sugiyama , T. Kimura
ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986 Volume 14 Issue 2

A highly integrated array processor (AAP2)-LSI has been developed. After the past 3 years study on the adaptive array processor 1 (AAP1), a challenging improvements on the SIMD's restraints are achieved by using the AAP2-LSI. The AAP2 array system makes it possible to carry out wideband modifiable operation (pseudo MIMD). Furthermore, each PE is capable of supporting a large amount of memory. The AAP2 potential for massively, parallel and pipelined processing is discussed in the field of im ...

12 Performance analysis of four SIMD machines 77%

Rod Fatoohi
Proceedings of the 7th international conference on Supercomputing August 1993

This paper presents the results of an experiment to study the performance of four SIMD machines. The objectives of this study are to analyze the cost of regular communication on several SIMD machines and study its impact on the performance of two kernels. The machines are: a 32k processor CM2, a 16k processor MPP, a 16k processor MasPar MP-1, and a 4k processor DAP 610C. Regular communication is exemplified, in this study, by the shift operation where all elements of an array are shifted so ...

13 IXM2 77%

Tetsuya Higuchi , Tatsumi Furuya , Kenichi Handa , Naoto Takahashi , Hiroyasu Nishiyama , Akio Kokubu
ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture April 1991 Volume 19 Issue 3

14 A symbolic substitution based parallel architecture and algorithms for high-speed parallel processing 77%

Ahmed Louri
Proceedings of the 1990 ACM annual conference on Cooperation January 1990

A new parallel architecture that is amenable to optical implementation is presented for massively data-parallel computing. The architecture is an SIMD model that exploits spatial parallelism and processes 2-D binary images as fundamental computational entities. Processing is based on a new technique called symbolic substitution logic. A hierarchical mapping technique is presented for designing data-parallel algorithms and mapping them onto the optical architecture. The mapp ...

Results 1 - 14 of 14 **short listing**

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2002 ACM, Inc.

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced

Member Services

- Join IEEE
- Establish IEEE Web Account

Print Format

Your search matched **22** of **784832** documents.
Results are shown **25** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the te
Then click **Search Again**.

(mpp or array processor) and bit serial

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Massively parallel inner-product array processor**
Genov, R.; Cauwenberghs, G.
Neural Networks, 2001. Proceedings. IJCNN '01. International Joint Conferer
Volume: 1 , 2001
Page(s): 183 -188 vol.1

[Abstract] [PDF Full-Text (504 KB)] **CNF**

2 **Charge-mode parallel architecture for vector-matrix multiplication**
Genov, R.; Cauwenberghs, G.
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transact
Volume: 48 Issue: 10 , Oct. 2001
Page(s): 930 -936

[Abstract] [PDF Full-Text (205 KB)] **JNL**

3 **Non-synchronous control of bit-serial video signal processor array architectures**
Riocreux, P.A.; Yates, R.B.
Image Processing, 1996. Proceedings., International Conference on , Volume
Page(s): 165 -168 vol.2

[Abstract] [PDF Full-Text (376 KB)] **CNF**

4 **Fast linear Hough transform**
Vuillemin, J.E.
Application Specific Array Processors, 1994. Proceedings. International Conf

1994
Page(s): 1 -9

[Abstract] [PDF Full-Text (352 KB)] **CNF**

---

5 **A compact array processor based on self-timed simultaneous bidir signalling**
Yacoub, G.Y.; Soni, T.; Ku, W.H.
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposiun 1993
Page(s): 1893 -1896 vol.3

[Abstract] [PDF Full-Text (336 KB)] **CNF**

---

6 **Digit systolic algorithms for fine-grain architectures**
Nagendra, C.; Owens, R.M.; Irwin, M.J.
Application-Specific Array Processors, 1993. Proceedings., International Con , 1993
Page(s): 466 -477

[Abstract] [PDF Full-Text (548 KB)] **CNF**

---

7 **GENES IV: A bit-serial processing element for a built-model neural accelerator**
Ienne, P.; Viredaz, M.A.
Application-Specific Array Processors, 1993. Proceedings., International Con , 1993
Page(s): 345 -356

[Abstract] [PDF Full-Text (540 KB)] **CNF**

---

8 **2-D discrete cosine transform array processor using non-planar co**

Ko, C.; Chung, W.
Data Compression Conference, 1991. DCC '91. , 1991
Page(s): 456

[Abstract] [PDF Full-Text (48 KB)] **CNF**

---

9 **A sliding memory array processor for low level vision**
Sunwoo, M.H.; Aggarwal, J.K.
Pattern Recognition, 1990. Proceedings., 10th International Conference on , , 1990
Page(s): 312 -317 vol.2

[Abstract] [PDF Full-Text (504 KB)] **CNF**

---

10 **PASIC. A sensor/processor array for computer vision**
Chen, K.; Danielsson, P.E.; Astrom, A.
Application Specific Array Processors, 1990. Proceedings of the International Conference on , 1990
Page(s): 352 -366

[Abstract] [PDF Full-Text (472 KB)] **CNF**

---

11 **Byte-serial convolvers**
Dadda, L.
Application Specific Array Processors, 1990. Proceedings of the International Conference on , 1990
Page(s): 530 -541

[Abstract] [PDF Full-Text (476 KB)] **CNF**

---

12 **The bit-serial systolic back-projection engine (BSSBPE)**
Bayford, R.
Application Specific Array Processors, 1990. Proceedings of the International Conference on , 1990
Page(s): 43 -54

[Abstract] [PDF Full-Text (344 KB)] **CNF**

---

13 **Digit-serial DSP architectures**
Parhi, K.K.; Wang, C.Y.
Application Specific Array Processors, 1990. Proceedings of the International Conference on , 1990
Page(s): 341 -351

[Abstract] [PDF Full-Text (412 KB)] **CNF**

---

14 **A multiple-level heterogeneous architecture for image understand**
Shu, D.B.; Nash, J.G.; Weems, C.C.
Application Specific Array Processors, 1990. Proceedings of the International Conference on , 1990
Page(s): 615 -627

[Abstract] [PDF Full-Text (608 KB)] **CNF**

---

15 **Use of A*N+B codes for fault-tolerant bit-serial array processors**
Piuri, V.
Computers and Communications, 1989. Conference Proceedings., Eighth Ani International Phoenix Conference on , 1989
Page(s): 9 -13

[Abstract] [PDF Full-Text (504 KB)] **CNF**

16 **Applications Of The Martin Marietta Single Module Advanced Syste Processor**
Haug, A.; Graybill, R.
Signals, Systems and Computers, 1988. Twenty-Second Asilomar Conferenc
Volume: 1 , 1988
Page(s): 189 -193

[Abstract] [PDF Full-Text (348 KB)] **CNF**

17 **CESAR-A programmable high performance systolic array processo**
Toverud, M.; Anderson, V.
Computer Design: VLSI in Computers and Processors, 1988. ICCD '88., Proc the 1988 IEEE International Conference on , 1988
Page(s): 414 -417

[Abstract] [PDF Full-Text (284 KB)] **CNF**

18 **A massively parallel systolic array processor system**
Morley, R.E., Jr.; Sullivan, T.J.
Systolic Arrays, 1988., Proceedings of the International Conference on , 198
Page(s): 217 -225

[Abstract] [PDF Full-Text (436 KB)] **CNF**

19 **The design of a bit-serial coprocessor to perform multiplication an division on a massively parallel architecture**
Morley, R.E., Jr.; Christensen, G.E.; Sullivan, T.J.; Kamin, O.
Frontiers of Massively Parallel Computation, 1988. Proceedings., 2nd Sympo the Frontiers of , 1989
Page(s): 419 -422

[Abstract] [PDF Full-Text (236 KB)] **CNF**

20 **BLITZEN: a highly integrated massively parallel machine**
Blevins, D.W.; Davis, E.W.; Heaton, R.A.; Reif, J.H.
Frontiers of Massively Parallel Computation, 1988. Proceedings., 2nd Sympo

the Frontiers of , 1989
Page(s): 399 -406

[Abstract] [PDF Full-Text (532 KB)] **CNF**

---

21 **The Martin Marietta advanced systolic array processor**
Haug, A.; Graybill, R.
Frontiers of Massively Parallel Computation, 1988. Proceedings., 2nd Sympo
the Frontiers of , 1989
Page(s): 367 -372

[Abstract] [PDF Full-Text (296 KB)] **CNF**

---

22 **New data movement algorithms for processor arrays**
Soraghan, J.J.
Acoustics, Speech, and Signal Processing, 1988. ICASSP-88., 1988 Internati
Conference on , 1988
Page(s): 1930 -1933 vol.3

[Abstract] [PDF Full-Text (268 KB)] **CNF**

Copyright © 2002 IEEE — All rights reserved

Search report

Set	Items	Description
S1	110	AU=(KIRSCH, G? OR KIRSCH G?)
S2	9	S1 AND IC=G06F?
S3	9	IDPAT (sorted in duplicate/non-duplicate order)
S4	5	IDPAT (primary/non-duplicate records only)

File 347:JAPIO Oct 1976-2002/Mar(Updated 020702)
(c) 2002 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2002/Jul W03
(c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020725,UT=20020718
(c) 2002 WIPO/Univentio
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200248
(c) 2002 Thomson Derwent

4/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014519001 **Image available**
WPI Acc No: 2002-339704/200237
XRPX Acc No: N02-267131

Active memory device for computer memory devices has connection circuit in which multiple PEs share their connection to multiple data bits in the memory array

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: **KIRSCH G**
Number of Countries: 096 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200219129	A2	20020307	WO 2001US27047	A	20010831	200237	B

Priority Applications (No Type Date): US 2000652003 A 20000831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200219129	A2	E	51	G06F-015/16	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

Abstract (Basic): WO 200219129 A2

NOVELTY - The memory includes a main memory and several processing elements. Each of the processing elements is coupled to a respective portion of the main memory by a single bit connection. A circuit is coupled between the main memory and the processing elements.

The circuit writes data from the processing elements to the memory in a horizontal mode and reads data stored in the main memory in a horizontal mode from the main memory to the processing elements.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a memory device, for a circuit for connecting a memory device and a processing element of an active memory, for a processing system and for a method for writing data from a processing element to a memory device.

USE - For computer memory devices.

ADVANTAGE - Provides connection between a PE array and main memory in an MPP such that software data conversion is not required and data can be stored in a normal mode or vertical mode in the memory.

DESCRIPTION OF DRAWING(S) - The figure shows a connection between a PE array and a memory.

pp; 51 DwgNo 5/7

Title Terms: ACTIVE; MEMORY; DEVICE; COMPUTER; MEMORY; DEVICE; CONNECT; CIRCUIT; MULTIPLE; PES; SHARE; CONNECT; MULTIPLE; DATA; BIT; MEMORY; ARRAY
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

4/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012841041 **Image available**
WPI Acc No: 2000-012873/200001

XRPX Acc No: N00-009985
Control logic designing system for complex digital system
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: **KIRSCH G**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5987239	A	19991116	US 96766650	A	19961213	200001	B

Priority Applications (No Type Date): US 96766650 A 19961213
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5987239	A		13	G06F-017/50	

Abstract (Basic): US 5987239 A
NOVELTY - A preprocessor combines skeleton file with one or more macrofiles to form output file. The preprocessor (32) processes or conditions the source code before it is passed onto compiler. The skeleton file, macrofiles and output file are stored in memory of computer system.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for control logic designing method for building a hardware description language.
USE - For complex digital system represented in hardware description language.
ADVANTAGE - The creation of single monolithic hardware description language source code file containing repetitions segments of microcode, is avoided by facilitating control logic design for a complex digital system.
DESCRIPTION OF DRAWING(S) - The figure shows a flow diagram describing the operation of preprocessor.
Preprocessor (32)
pp; 13 DwgNo 3/5
Title Terms: CONTROL; LOGIC; DESIGN; SYSTEM; COMPLEX; DIGITAL; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

4/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012829977 **Image available**
WPI Acc No: 2000-001809/200001
Related WPI Acc No: 1999-622401
XRPX Acc No: N00-001565
Processor with in-circuit emulation e.g. for system development
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: KERSHAW S; **KIRSCH G** ; KERSHAW S M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2338320	A	19991215	GB 9812512	A	19980610	200001	B
US 6385742	B1	20020507	US 99262816	A	19990305	200235	

Priority Applications (No Type Date): GB 984910 A 19980306
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2338320	A		14	G06F-011/00	
US 6385742	B1			G06F-011/28	

Abstract (Basic): GB 2338320 A

NOVELTY - The processor uses a series of scan-chains serially connected registers coupled to a serial scanning unit to execute the emulation. The first scan-chain includes an address register (16) for providing an address on an address bus to memory (14). The address register value is incremented by the processor. The scan-chains are arranged to control the processor incrementation, whilst a second scan-chain includes a data register coupled to the data bus (91) of the memory to read/write data.

DETAILED DESCRIPTION - The output of the data register is coupled to an incrementor via an address multiplexer (102), which in turn is controlled by the microcode register. Memory access for debugging is made practicable by limiting the number of operations needed for each access.

An INDEPENDENT CLAIM is include for a method of in-circuit emulation for a processor.

USE - Processor with in-circuit emulation, for carrying out debugging operations during development.

ADVANTAGE - The processor development system can access memory for debugging without creating undue demands on the memory for this operation, thus preventing undue delays.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the processor.

Synchronous memory (14)
Address register (16)
Data bus (91)
Address multiplexer (102)
pp; 14 DwgNo 1/2

Title Terms: PROCESSOR; CIRCUIT; EMULATION; SYSTEM; DEVELOP
Derwent Class: T01
International Patent Class (Main): **G06F-011/00 ; G06F-011/28**
International Patent Class (Additional): **G06F-009/455**
File Segment: EPI

4/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012816170 **Image available**
WPI Acc No: 1999-622401/199954
Related WPI Acc No: 2000-001809
XRPX Acc No: N99-459290

Software debugging in circuit emulation with scan chains for use in pipeline microprocessors

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: KERSHAW S; **KIRSCH G**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2337834	A	19991201	GB 984910	A	19980306	199954	B

Priority Applications (No Type Date): GB 984910 A 19980306
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2337834	A		17	G06F-011/00	

Abstract (Basic): GB 2337834 A

NOVELTY - The processor (40) to be debugged is provided with a chain of scan registers (16) and a breakpoint interrupt is either

detected or created (52). The processor completes it current instruction and sends a signal to the scan interface logic which asserts the start scan signal (48) on the clock control unit (46). The clock controller stops the processor clock and the external scan unit is alerted to start the scan sequence.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the method of carrying out debugging procedures on a processor with scan registers.

USE - For carrying out debugging procedures on a processor, especially suited to pipeline processors.

ADVANTAGE - A software debugging in circuit emulation session can be entered without the need to stop the processor clock during current actions. The pipeline is filled with no operation instructions (NOP) so that information in the pipeline is not lost.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the processor debugging apparatus.

Scan registers (16)
Processor (40)
Clock control unit (46)
Start scan signal (48)
Breakpoint interrupt (52)
pp; 17 DwgNo 4/7

Title Terms: SOFTWARE; DEBUG; CIRCUIT; EMULATION; SCAN; CHAIN; PIPE; MICROPROCESSOR
Derwent Class: T01
International Patent Class (Main): **G06F-011/00**
International Patent Class (Additional): **G06F-011/34**
File Segment: EPI

4/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012804397 **Image available**
WPI Acc No: 1999-610627/199952
XRPX Acc No: N99-449928

Debugging method for use in microprocessor development system

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: KERSHAW S; **KIRSCH G** ; SLADE B
Number of Countries: 084 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9948001	A1	19990923	WO 99GB840	A	19990318	199952	B
AU 9929464	A	19991011	AU 9929464	A	19990318	200008	

Priority Applications (No Type Date): GB 9810774 A 19980519; GB 985832 A 19980318
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9948001	A1	E	21	G06F-011/00	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9929464	A		G06F-011/00	Based on patent WO 9948001

Abstract (Basic): WO 9948001 A1
NOVELTY - A host computer system writes a program for reading

and/or writing data at a specified memory location corresponding to the memory mapped area of peripheral devices, into the memory (4) of a processor (2). The system enables the processor to run the stored program and then return to the debug process in which the data at specified location is written to host computer system.

DETAILED DESCRIPTION - The processor (2) includes in- circuit emulation unit with one or more scan chains (6) of serially connected registers (8) that are accessed by the external host computer system. The host computer system carries out debugging via scan chains and selectively interrupts debugging for accessing peripheral memory mapped device. The scan chains are connected to an interface (10) which is coupled to the host computer (12), and permits transfer of data and instructions during debugging or scanning. The host computer (12) includes a file (16) containing configuration information of selected registers of the target processor, based on which the host computer selectively configures predetermined registers of the processor for the program to be run by the processor.

USE - For debugging host computer in microprocessor development system.

ADVANTAGE - Reduces cost since memory space required for storing monitor program, is reduced. Permits complete observation of working of microprocessor since the microprocessor's registers are coupled together in series to form one or more test chains which can be accessed by external host to load test data and to read out the results in a serial manner. Once the data transfer is complete, the back-up data and program RAM contents are loaded back into the quantity of RAM and execution can be continued normally, hence the need for complex logic is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows schematic block diagram of debug system and target processor.

Processor (2)
Memory (4)
Scan chains (6)
Register (8)
Interface (10)
Host computer (12)
File (16)

pp; 21 DwgNo 1/6

Title Terms: DEBUG; METHOD; MICROPROCESSOR; DEVELOP; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-011/00**
File Segment: EPI

Search report

Set	Items	Description
S1	19546	MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCESSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGEMENT? OR ORDER OR FORMATION)
S2	28168	(SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N)(CONNECT? OR LINK?) OR SINGLE()BIT
S3	2191	MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?)
S4	12790	MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5	608	MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6	734	VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7	1075026	VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8	1094350	HORIZONTAL? OR ROW OR NORMAL?
S9	359717	BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE
S10	0	S1 AND S2 AND S3 AND S4 AND S5 AND S6
S11	32	S1 AND S2
S12	0	S3 AND S4 AND S5 AND S6
S13	2	S3 AND S4 AND S5
S14	0	S1 AND S6
S15	2	S2 AND S6
S16	1	S11 AND S3
S17	2	S11 AND S4
S18	0	S11 AND S5
S19	0	S11 AND S6
S20	47682	S1 OR S2
S21	11	S20 AND S3
S22	72	S20 AND S4
S23	1	S20 AND S5
S24	2	S20 AND S6
S25	81	S21 OR S22 OR S33 OR S24
S26	31	S25 AND IC=G06F?
S27	59	S20 AND S7 AND S8 AND S9
S28	10	S27 AND IC=G06F?
S29	10	S28 NOT S26
S30	41	S26 OR S28
S31	41	IDPAT (sorted in duplicate/non-duplicate order)
S32	41	IDPAT (primary/non-duplicate records only)

File 347:JAPIO Oct 1976-2002/Mar(Updated 020702)
(c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200247
(c) 2002 Thomson Derwent

32/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014622819 **Image available**
WPI Acc No: 2002-443523/200247
XRPX Acc No: N02-349456
Interface device has physical layer which outputs standby signal in active state to optical transceiver to change transceiver from normal **operation** mode **to low power consumption mode**
Patent Assignee: NEC CORP (NIDE)
Inventor: TAKEUCHI J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020046355	A1	20020418	US 2001970529	A	20011004	200247	B
JP 2002118563	A	20020419	JP 2000306704	A	20001005	200247	

Priority Applications (No Type Date): JP 2000306704 A 20001005
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020046355	A1		26	G06F-001/26	
JP 2002118563	A		16	H04L-012/28	

Abstract (Basic): US 20020046355 A1
NOVELTY - A physical layer (10) outputs a standby signal in an active state to an optical transceiver (30) to change the transceiver from **normal** operation **mode** to low power consumption mode, when the physical layer is in low power consumption mode.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for interface device power control method.
USE - Interface device.
ADVANTAGE - The transition of optical transceiver to low power consumption mode, when the physical layer is in low power consumption mode, enables reduction in the power consumption of the device.
DESCRIPTION OF DRAWING(S) - The figure shows the configuration of the interface device.
Physical layer (10)
Optical transceiver (30)
pp; 26 DwgNo 1/14
Title Terms: INTERFACE; DEVICE; PHYSICAL; LAYER; OUTPUT; STANDBY; SIGNAL; ACTIVE; STATE; OPTICAL; TRANSCEIVER; CHANGE; TRANSCEIVER; NORMAL; OPERATE ; MODE; LOW; POWER; CONSUME; MODE
Derwent Class: T01; U12; W01; W02
International Patent Class (Main): **G06F-001/26** ; H04L-012/28
International Patent Class (Additional): **G06F-001/32** ; H04B-001/40; H04B-007/26; H04B-010/20; H04L-029/00
File Segment: EPI

32/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014519001 **Image available**
WPI Acc No: 2002-339704/200237
XRPX Acc No: N02-267131
Active memory device for computer memory devices has connection circuit in which multiple PEs share their connection to multiple data bits in the memory array
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: KIRSCH G
Number of Countries: 096 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200219129	A2	20020307	WO 2001US27047	A	20010831	200237	B

Priority Applications (No Type Date): US 2000652003 A 20000831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200219129	A2	E	51	G06F-015/16	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

Abstract (Basic): WO 200219129 A2

NOVELTY - The memory includes a main memory and several processing elements. Each of the processing elements is coupled to a respective portion of the main memory by a **single bit** connection. A circuit is coupled between the main memory and the processing elements.

The circuit writes data from the processing elements to the memory in a **horizontal mode** and reads data stored in the main memory in a **horizontal mode** from the main memory to the processing elements.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a memory device, for a circuit for connecting a memory device and a processing element of an active memory, for a processing system and for a method for writing data from a processing element to a memory device.

USE - For computer memory devices.

ADVANTAGE - Provides connection between a **PE** array and main memory in an **MPP** such that software data conversion is not required and data can be stored in a **normal mode** or **vertical mode** in the memory.

DESCRIPTION OF DRAWING(S) - The figure shows a connection between a **PE** array and a memory.

pp; 51 DwgNo 5/7

Title Terms: ACTIVE; MEMORY; DEVICE; COMPUTER; MEMORY; DEVICE; CONNECT; CIRCUIT; MULTIPLE; PES; SHARE; CONNECT; MULTIPLE; DATA; BIT; MEMORY; ARRAY
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

32/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

014375290 **Image available**
WPI Acc No: 2002-195993/200225
XRPX Acc No: N02-148848

Microcode multi-way branching system e.g. for microprocessors, utilizes a technique of microprocessed control which divides all instructions into normal '' **and xway** modes

Patent Assignee: UNISYS CORP (BURS)
Inventor: CRISWELL P B; PETERSON E R
Number of Countries: 020 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200210913	A1	20020207	WO 2001US21642	A	20010709	200225	B

Priority Applications (No Type Date): US 2000626030 A 20000727
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200210913 A1 E 22 G06F-009/28
Designated States (National): JP
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Abstract (Basic): WO 200210913 A1
NOVELTY - Data processing system has an instruction processor which is implemented using a microprogrammed and pipelined architecture comprises: a **normal modes** ; an xway **mode** ; and a microprogramming bit which defines between the **normal mode** and the xway mode.
DETAILED DESCRIPTION - INDEPENDENT CLAIM is also included for the following:apparatus; method of processing a branch instruction
USE - For microprocessors.
ADVANTAGE - Provides branch control information one cycle earlier than found in conventional systems. This overcomes the latency involved in reading the control information from the microcode RAM. Thus, the system can branch on every machine cycle rather than on every other machine cycle. The number of bits required of the microcode is limited through the use of a Look Up Table (LUT).
DESCRIPTION OF DRAWING(S) - The diagram shows the system with microcode multi-way branching capability
single bit position (112)
look up table (102)
pp; 22 DwgNo 2/4
Title Terms: MULTI; WAY; BRANCH; SYSTEM; MICROPROCESSOR; TECHNIQUE; CONTROL ; DIVIDE; INSTRUCTION; NORMAL; MODE
Derwent Class: T01
International Patent Class (Main): **G06F-009/28**
International Patent Class (Additional): **G06F-009/26**
File Segment: EPI

32/5/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

013990110 **Image available**
WPI Acc No: 2001-474324/200151
Palm sized portable computer for operating poniter of computer system
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM J S
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
KR 2001011369 A 20010215 KR 9930689 A 19990727 200151 B

Priority Applications (No Type Date): KR 9930689 A 19990727
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
KR 2001011369 A 1 G06F-003/033

Abstract (Basic): KR 2001011369 A
NOVELTY - A palm sized portable computer is provided to elaborately move a pointer on a screen of a computer system, for example in a graphic application program.
DETAILED DESCRIPTION - A palm sized portable computer(200) comprises a stylus pen(210), a TSP(Touch Sensitive Panel, 220), a TSP interface(230), a memory(240), a CPU(250), an I/O controller(260) and a

serial port(270). The palm sized portable computer has a **normal mode** for performing a general computer function, and a pointing mode for moving a pointer on a display unit of a computer system(100). The normal node or the pointing mode can be selected by a user pushing a button displayed on the TSP(220) with the stylus pen(210). The serial port(270) is **connected** to a **serial** port of the computer system(100) for a data transmission. In the case that the palm sized portable computer is in the pointing mode, the data transmitted via the serial port(270) is a pointing data. The computer system displays the pointer on the display unit of the computer system according to the pointing data transmitted from the palm sized portable computer(200).

pp; 1 DwgNo 1/10

Title Terms: PALM; SIZE; PORTABLE; COMPUTER; OPERATE; COMPUTER; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-003/033**
File Segment: EPI

32/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

013835374 **Image available**
WPI Acc No: 2001-319586/200134
Related WPI Acc No: 1998-243559; 2001-319585
XRPX Acc No: N01-229769

Reprogramming a microprocessor through a serial port, where control of a microprocessor is achieved by a sequence of signals transmitted from an administrative computer through a serial port

Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: OLIVER J A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2355326	A	20010418	GB 9719882	A	19970919	200134	B
			GB 2001718	A	20010111		
GB 2355326	B	20010711	GB 9719882	A	19970919	200140	
			GB 2001718	A	20010111		

Priority Applications (No Type Date): US 96719936 A 19960925
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2355326	A		20	G06F-009/445	Derived from application GB 9719882
GB 2355326	B			G06F-009/445	Derived from application GB 9719882

Abstract (Basic): GB 2355326 A

NOVELTY - Administrative computer is **connected** to a **serial** port (18) on a machine (12) containing a microprocessor (30) or some other memory device to be reprogrammed. A sequence of signals is sent from the administrative computer to the microprocessor, via control grabber hardware circuit (28), to change the microprocessor from a **normal mode** to a bootstrap mode. A new program is then loaded from the administrative computer, and a second signal sequence is sent to reset the microprocessor. Both digital and analogue implementations of the control grabber circuit (28), which constantly monitors the state of handshake and receive data lines and identifies the proper sequence of signals, are described

DETAILED DESCRIPTION - INDEPENDENT CLAIM is also included for the following:

(a) apparatus containing microprocessor

USE - For microprocessors.

ADVANTAGE - Reconfigures a programmable microprocessor using an existing interface without disassembly of the equipment containing the microprocessor.

DESCRIPTION OF DRAWING(S) - The diagram shows the system for reprogramming a microprocessor

microprocessor (30)

serial port (18)

control grabber hardware (28)

pp; 20 DwgNo 2/10

Title Terms: REPROGRAMMABLE; MICROPROCESSOR; THROUGH; SERIAL; PORT; CONTROL ; MICROPROCESSOR; ACHIEVE; SEQUENCE; SIGNAL; TRANSMIT; ADMINISTER; COMPUTER; THROUGH; SERIAL; PORT

Derwent Class: T01; U21

International Patent Class (Main): **G06F-009/445**

File Segment: EPI

32/5/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

013835373 **Image available**

WPI Acc No: 2001-319585/200134

Related WPI Acc No: 1998-243559; 2001-319586

XRPX Acc No: N01-229768

Reprogramming a microprocessor through a serial port, where administrative computer sends a sequence of signals to the microprocessor to activate a preinstalled program on the microprocessor

Patent Assignee: EASTMAN KODAK CO (EAST)

Inventor: OLIVER J A

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2355325	A	20010418	GB 9719882	A	19970919	200134	B
			GB 2001707	A	20010111		
GB 2355325	B	20010711	GB 9719882	A	19970919	200140	
			GB 2001707	A	20010111		

Priority Applications (No Type Date): US 96719936 A 19960925

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2355325	A		19	G06F-009/445	Derived from application GB 9719882
GB 2355325	B			G06F-009/445	Derived from application GB 9719882

Abstract (Basic): GB 2355325 A

NOVELTY - Administrative computer (14) is **connected** to a **serial** port (18) on a machine (12) containing a microprocessor (30) or some other memory device to be reprogrammed. A sequence of signals is sent from the administrative computer to the microprocessor, via control grabber hardware circuit (28), to change the microprocessor from a **normal mode** to a bootstrap mode. A new program is then loaded from the administrative computer, and a second signal sequence is sent to reset the microprocessor. Both digital and analogue implementations of the control grabber circuit (28), which constantly monitors the state of handshake and receive data lines and identifies the proper sequence of signals, are described.

USE - For microprocessors.

ADVANTAGE - Reconfigures a programmable microprocessor using an existing interface without disassembly of the equipment containing the

microprocessor.
DESCRIPTION OF DRAWING(S) - The diagram shows the system for reprogramming a microprocessor
microprocessor (30)
serial port (18)
control grabber hardware (28)
pp; 19 DwgNo 2/10
Title Terms: REPROGRAMMABLE; MICROPROCESSOR; THROUGH; SERIAL; PORT; ADMINISTER; COMPUTER; SEND; SEQUENCE; SIGNAL; MICROPROCESSOR; ACTIVATE; PROGRAM; MICROPROCESSOR
Derwent Class: T01; U21
International Patent Class (Main): **G06F-009/445**
File Segment: EPI

32/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

012298323 **Image available**
WPI Acc No: 1999-104429/199909
XRPX Acc No: N99-075367
Diagnostic RAM mode for RAM limited microcontroller based applications - uses re-definition of RAM for special mode with data produce read via a serial link **, the normal operation being curtailed during the procedure**
Patent Assignee: ANONYMOUS (ANON)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RD 417011	A	19990110	RD 98417011	A	19981220	199909	B

Priority Applications (No Type Date): RD 98417011 A 19981220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RD 417011	A		1	G06F-000/00	

Abstract (Basic): RD 417011 A
The special diagnostics RAM mode is redefined from the RAM definition constructed during **normal** operation. The **mode** allows for mirroring of EEPROM data in to RAM in pages of blocks of 64 or 128 bytes depending on available RAM. The data is read then available to read via a **serial link** . Normal operation is curtailed during this mode and a part reset is executed upon completion.
ADVANTAGE - Allows user access to data stored in external EEPROM in RAM limited microcontroller based applications.
Dwg.1/1
Title Terms: DIAGNOSE; RAM; MODE; RAM; LIMIT; BASED; APPLY; DEFINE; RAM; SPECIAL; MODE; DATA; PRODUCE; READ; SERIAL; LINK; NORMAL; OPERATE; PROCEDURE
Derwent Class: T01
International Patent Class (Main): **G06F-000/00**
File Segment: EPI

32/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

011826649 **Image available**
WPI Acc No: 1998-243559/199822
Related WPI Acc No: 2001-319585; 2001-319586

XRPX Acc No: N98-192802

Remote microprocessor reprogramming via serial port - involves sending signal sequence from administrative computer to microprocessor followed by loading new program

Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: OLIVER J A
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2319365	A	19980520	GB 9719882	A	19970919	199822	B
JP 10207703	A	19980807	JP 97259887	A	19970925	199842	
US 5913056	A	19990615	US 96719936	A	19960925	199930	
GB 2319365	B	20010711	GB 9719882	A	19970919	200140	

Priority Applications (No Type Date): US 96719936 A 19960925
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2319365	A		22	G06F-009/445	
JP 10207703	A		8	G06F-009/06	
US 5913056	A			G06F-009/00	
GB 2319365	B			G06F-009/445	

Abstract (Basic): GB 2319365 A

The reprogramming method involves connecting an administrative computer to a serial cable. The serial cable is then **connected** to the **serial** port on a machine containing the microprocessor. A fist sequence of signals is sent form the administrative computer to the microprocessor to change the microprocessor from a **normal** to a bootstrap **mode** .

A new program is loaded from the administrative computer to the microprocessor. A second sequence of signals is sent from the administrative computer to the microprocessor to reset it. A reset signal is rescinded prior to loading the new program.

ADVANTAGE - Provides low cost, simple and reliable interface avoiding use of floppy or tape drive to load data.

Dwg.8/10

Title Terms: REMOTE; MICROPROCESSOR; REPROGRAMMABLE; SERIAL; PORT; SEND; SIGNAL; SEQUENCE; ADMINISTER; COMPUTER; MICROPROCESSOR; FOLLOW; LOAD; NEW ; PROGRAM
Derwent Class: T01
International Patent Class (Main): **G06F-009/00 ; G06F-009/06 ; G06F-009/445**
File Segment: EPI

32/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

011444112 **Image available**
WPI Acc No: 1997-422019/199739
Related WPI Acc No: 1998-008295
XRPX Acc No: N97-351511

Data communication system of computer - has communication control unit that controls sending of data between processors through input-output ports

Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9190421	A	19970722	JP 8963091	A	19890314	199739	B

JP 9731984 A 19890314

Priority Applications (No Type Date): JP 8963091 A 19890314; JP 9731984 A 19890314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9190421	A		7	G06F-015/80	Div ex application JP 8963091

Abstract (Basic): JP 9190421 A

The system consists of a number of processors (**PE**) arranged in a matrix, connected **horizontally** and **vertically** by **horizontal** and **vertical** wires respectively. Every processor is connected to four adjacent processors on all direction with a communication control part, using four **bi - directional** input-output ports. A memory unit of one word length is provided. Four input sides of input registers (r) along with data processing unit forms a unification control circuit and four output sides of output registers (r) along with data processing unit forms a branching control circuit.

A communication control unit obtains data from the processor or from adjacent processors through the unification control circuit and controls to send data through the branching control circuit to adjacent processors.

ADVANTAGE - Reduces size by limiting number of pins and distance between processors. Avoids dead lock. Aids in easy mounting.

Dwg.1/5

Title Terms: DATA; COMMUNICATE; SYSTEM; COMPUTER; COMMUNICATE; CONTROL; UNIT; CONTROL; SEND; DATA; PROCESSOR; THROUGH; INPUT; OUTPUT; PORT
Derwent Class: T01
International Patent Class (Main): **G06F-015/80**
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

32/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

010644236 **Image available**
WPI Acc No: 1996-141190/199615
XRPX Acc No: N96-118201

Electronic document viewer - includes navigator which permits display of next and remaining sequential portions of article in content flow or reverse content flow order

Patent Assignee: ADOBE SYSTEMS INC (ADOB-N)
Inventor: COHN R J; MCCOY W H; PADGETT A P; WARNOCK J E
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 701220	A1	19960313	EP 95305286	A	19950728	199615	B
CA 2154951	A	19960313	CA 2154951	A	19950728	199626	
JP 8190547	A	19960723	JP 95234321	A	19950912	199639	
US 5634064	A	19970527	US 94304680	A	19940912	199727	
			US 96693489	A	19960802		
EP 701220	B1	20010704	EP 95305286	A	19950728	200138	
DE 69521575	E	20010809	DE 621575	A	19950728	200153	
			EP 95305286	A	19950728		

Priority Applications (No Type Date): US 94304680 A 19940912; US 96693489 A 19960802
Cited Patents: 04Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 701220	A1	E	31	G06F-017/21	
Designated States (Regional): DE FR GB IT NL SE					
CA 2154951	A			G06F-003/14	
JP 8190547	A		49	G06F-017/21	
US 5634064	A		28	G06T-001/00	Cont of application US 94304680
EP 701220	B1	E		G06F-017/21	
Designated States (Regional): DE FR GB IT NL SE					
DE 69521575	E			G06F-017/21	Based on patent EP 701220

Abstract (Basic): EP 701220 A

The document viewer includes a computer system with digital processor, memory which provides memory storage locations accessible by the digital processor, a visual output device to provide a visual output derived, at least in part, from the digital processor, and an input device to provide an input that can be acted upon by the digital processor. A document stored in the memory includes article section information and section link information describing an ordering of the article sections such that the article sections can be accessed in a consecutive fashion.

One of a number of view modes including at least a **normal** view **mode** and an article view **mode** is determined. The **normal** view device displays a portion of the document on the visual output device in a normal view that does not require the article section information and article section link information. The article view device displays portions of a selected article in an article view, and permits the sequential viewing of consecutive article sections of the selected article based upon the section link information.

ADVANTAGE - Reader can follow thread of article in convenient, easily comprehendible fashion.

Dwg.1/8

Title Terms: ELECTRONIC; DOCUMENT; VIEW; NAVIGATION; PERMIT; DISPLAY; REMAINING; SEQUENCE; PORTION; ARTICLE; CONTENT; FLOW; REVERSE; CONTENT; FLOW; ORDER

Derwent Class: T01

International Patent Class (Main): **G06F-003/14 ; G06F-017/21 ;** G06T-001/00

International Patent Class (Additional): **G06F-017/24**

File Segment: EPI

32/5/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

010401114 **Image available**

WPI Acc No: 1995-302427/199539

XRPX Acc No: N95-229650

Software down-loading system for transferring software from remote programmer to Electronic Engine Control unit - enables remote programmer to select 1st mode, in which programmer down-loads boot program through serial channel into shared memory, 2nd mode, in which CPU executes code in shared memory or 3rd mode in which CPU controls serial channel

Patent Assignee: UNITED TECHNOLOGIES CORP (UNAC)

Inventor: ADAMEC W B; COX R E; GIGANDET S A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5444861	A	19950822	US 92890776	A	19920601	199539	B
			US 94317984	A	19941004		

Priority Applications (No Type Date): US 92890776 A 19920601; US 94317984 A 19941004
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5444861	A		8	G06F-015/16	Cont of application US 92890776

Abstract (Basic): US 5444861 A

A remote programmer communicates with the Electronic Engine Control unit through a **serial** communications **link** . The Electronic Engine Control unit receives the communications through a serial memory that transmits them to a shared memory and on through a central processing unit - CPU - to a program memory. A redundant control circuit is controlled by the remote programmer and directs the EEC unit through three operational modes.

In a first, or down-load/verify, mode of operation, the EEC unit may receive and store a boot program. In a second, or program memory, mode, the CPU executes the boot program to allow the CPU to read from and/or write to the program memory in response to communications from the serial channel. In a third, or **normal** , **mode** of operation, the CPU can only read from the program memory and an on-board or host computer may replace the remote programmer, so that the CPU executes software stored in the program memory in response to communications received from the host computer to control multiple actuators on the engines, but the host computer cannot access the EEC unit's program memory.

USE/ADVANTAGE - For down-loading, verifying, and/or testing software from remote programmer to Electronic Engine Control unit on gas turbine engine for controlling engine functions such as fuel supply using throttle valve. Uses min. no. of electrical connector fixtures within container housing components of unit. Enables software to be changed, verified and/or tested without opening container, or removing any component. Prevents access to software loaded into program memory during ordinary usage of unit.

Dwg.2/4

Title Terms: SOFTWARE; DOWN; LOAD; SYSTEM; TRANSFER; SOFTWARE; REMOTE; PROGRAM; ELECTRONIC; ENGINE; CONTROL; UNIT; ENABLE; REMOTE; PROGRAM; SELECT; MODE; PROGRAM; DOWN; LOAD; BOOT; PROGRAM; THROUGH; SERIAL; CHANNEL; SHARE; MEMORY; MODE; CPU; EXECUTE; CODE; SHARE; MEMORY; MODE; CPU; CONTROL; SERIAL; CHANNEL
Derwent Class: T01; W06
International Patent Class (Main): **G06F-015/16**
International Patent Class (Additional): **G06F-009/06** ; **G06F-009/24**
File Segment: EPI

32/5/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

010346335 **Image available**
WPI Acc No: 1995-247649/199533
XRPX Acc No: N95-192326

Field service remote communication system for image setters or copiers - uses service centre computer to communicate with image setter to upload and download information with the image setter and to instruct it to perform diagnostics

Patent Assignee: BAYER CORP (FARB); MILES INC (MILE)
Inventor: CARLSON G L; VEIGA L F
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

EP 663623	A2	19950719	EP 94120417	A	19941222	199533	B
JP 7325734	A	19951212	JP 955337	A	19950117	199607	
EP 663623	A3	19961030	EP 94120417	A	19941222	199649	

Priority Applications (No Type Date): US 94182542 A 19940114
Cited Patents: No-SR.Pub; GB 2247540; US 5214772; WO 9213295
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 663623	A2	E	18	G03G-015/00	
Designated States (Regional): BE DE FR GB					
JP 7325734	A		11	G06F-011/30	
EP 663623	A3			G03G-015/00	

Abstract (Basic): EP 663623 A
The image setter (100) is **connected** via a **serial connection** (160) to a modem (110), which is connected through a telephone network connection (140) to another modem (120), which is connected to a field service computer (130). The computer is operated by a field service engineer who can be located anywhere in the world. The computer is housed in a service centre which has a database containing the telephone numbers of the installed image setters.
The computer initiates a call to an image setter and a data connection is established when the computer sends a signal for the image setter to enter the service **mode** , when it halts **normal** operations. The computer can then upload and download data to the image setter with the data being firmware, configuration data or error information. The image setter can request service and the computer can instruct the image setter to execute diagnostic testing to determine the status of the image setter.
ADVANTAGE - Automatic system which reduces servicing costs.
Dwg.1/10
Title Terms: FIELD; SERVICE; REMOTE; COMMUNICATE; SYSTEM; IMAGE; SET; COPY; SERVICE; CENTRE; COMPUTER; COMMUNICATE; IMAGE; SET; INFORMATION; IMAGE; SET; INSTRUCTION; PERFORMANCE; DIAGNOSE
Index Terms/Additional Words: maintenance
Derwent Class: P84; S06; T01; W01; W05
International Patent Class (Main): G03G-015/00; **G06F-011/30**
International Patent Class (Additional): G06T-001/00; G08B-025/08
File Segment: EPI; EngPI

32/5/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

010106544 **Image available**
WPI Acc No: 1995-007797/199502
XRPX Acc No: N95-006535
Shape recognition - comparing point series with master pattern represented by node points and connecting line elements
Patent Assignee: MATSUSHITA ELECTRIC WORKS LTD (MATW)
Inventor: FUJIWARA Y; IKEBUCHI H; MITAKA R; SHOTADASHI K; YOSHISUKE S; FIJIWARA Y
Number of Countries: 005 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4418217	A1	19941201	DE 4418217	A	19940525	199502	B
FR 2705809	A1	19941202	FR 946308	A	19940525	199503	
CA 2123530	A	19941127	CA 2123530	A	19940513	199509	
US 5546476	A	19960813	US 94242669	A	19940513	199638	
DE 4418217	C2	19960926	DE 4418217	A	19940525	199643	

CN 1106155	A	19950802	CN 94105487	A	19940526	199730	
CA 2123530	C	19990504	CA 2123530	A	19940513	199936	

Priority Applications (No Type Date): JP 946842 A 19940126; JP 93124508 A 19930526

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4418217	A1		49	G06K-009/46	
US 5546476	A		47	G06K-009/46	
DE 4418217	C2		49	G06K-009/46	
CA 2123530	C	E		G06K-009/62	
FR 2705809	A1			G06K-009/46	
CA 2123530	A			G06F-015/70	
CN 1106155	A			G06K-009/00	

Abstract (Basic): DE 4418217 A

A master shape is represented by a set contg. a limited number of node points and line elements which **successively** produce **connections** between the node points. A standard value and a tolerance implying the standard value are defined w.r.t. a characteristic of each line element.

The degree of coincidence of the shape with the shape pattern is determined on the basis of any deviation of the point series of the shape from the standard value and the relationship to the tolerance.

USE/ADVANTAGE - For identifying shape represented by series of points in two-dimensional plane by comparison with master shape. Enables shape recognition without altering master shape where input data are prepared sequentially and individual shapes vary.

Dwg.1/42

Title Terms: SHAPE; RECOGNISE; COMPARE; POINT; SERIES; MASTER; PATTERN; REPRESENT; NODE; POINT; CONNECT; LINE; ELEMENT

Derwent Class: S02; T04

International Patent Class (Main): **G06F-015/70** ; G06K-009/00; G06K-009/46; G06K-009/62

International Patent Class (Additional): G01B-011/00; G01B-011/03; G01B-011/24; **G06F-015/46** ; G06K-009/50; G06K-009/68; G06T-001/00

File Segment: EPI

32/5/14 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

009915185 **Image available**

WPI Acc No: 1994-182895/199422

XRPX Acc No: N94-144464

Linear equations calculation method using multiprocessor system - involves manipulating matrices and unknown vector values such that problem can be solved using vector orthogonalisation techniques

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: GUPTA S; MEHROTRA R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5319586	A	19940607	US 89458207	A	19891228	199422	B
			US 9318343	A	19930216		

Priority Applications (No Type Date): US 89458207 A 19891228; US 9318343 A 19930216

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

US 5319586 A 11 G06F-015/32 Cont of application US 89458207

Abstract (Basic): US 5319586 A

The method involves receiving the system of linear equations by the host processor, the host processor expressing the system of linear equations as a matrix having rows and **columns** of coefficient values. Each **row** is equal to a known constant. The coefficient values are transferred by the host processor to the **processor array** . The **processor array** is controlled to **normalize** a **row** of the matrix, to obtain a **normalized** vector and to modify the remaining rows of the matrix to obtain zero constant vectors. The zero constant vectors are **normalised** with respect to each other and then the **normalized** vector is orthogonalised with respect to the orthogonalized zero constant vectors, to obtain a **perpendicular** vector.

Orthogonalisation is performed by multiple processors of the **processor array** . A solution vector is obtained by the **processor array** as the product of a scaling factor and the **perpendicular** vector. The host processor receives the solution vector.

ADVANTAGE - Speeds up solution of system of linear equations and matrix inversion.

Dwg.1/5

Title Terms: LINEAR; EQUATE; CALCULATE; METHOD; MULTIPROCESSOR; SYSTEM; MANIPULATE; MATRIX; UNKNOWN; VECTOR; VALUE; PROBLEM; CAN; SOLVING; VECTOR ; TECHNIQUE

Derwent Class: T01

International Patent Class (Main): **G06F-015/32**

International Patent Class (Additional): **G06F-007/00**

File Segment: EPI

32/5/15 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

009657558 **Image available**

WPI Acc No: 1993-351110/199344

XRPX Acc No: N93-270888

Signal indication switching method for controlling traffic signal indicators for control of traffic movements - using linear programming solutions for maximum, optimum and minimum cycle lengths and max, optimum and min. phase times

Patent Assignee: MITSUBISHI CORP (MITS)

Inventor: SAKITA M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5257194	A	19931026	US 91694013	A	19910430	199344	B

Priority Applications (No Type Date): US 91694013 A 19910430

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5257194	A		62	G06F-015/48	

Abstract (Basic): US 5257194 A

The traffic signal local control method is used to automatically compute, or adjust the signal timing for the prevailing traffic, not only from the local intersection control standpoint, but also from the area-wide signal control standpoint, when employed in an area-wide system of traffic control. The traffic signal local controller includes the use of time-of-day tables including signal control method, signal phasing scheme, recall switch, signal timing parameter and **pedestrian**

green time coefficient tables. Signal control methods which may be implemented include time-of-day failure **mode** , time-of-day **normal mode** , traffic-responsive and traffic-adaptive methods.

Signal phasing schemes are defined by data included in a transition matrix (P) and in a simultaneous green matrix (Q) included in time-of-day tables. The transition matrix (P) indicates which movement follows another, and the simultaneous green matrix contains data on simultaneous green indications.

USE/ADVANTAGE - Handling on-line real-time basis, many signal control functions performed by central computer and off-line analysis performed by traffic engineer. Flexible enough to accommodate most present, and future, traffic signal control, or optimisation methods.

Dwg.29/29f

Title Terms: SIGNAL; INDICATE; SWITCH; METHOD; CONTROL; TRAFFIC; SIGNAL; INDICATE; CONTROL; TRAFFIC; MOVEMENT; LINEAR; PROGRAM; SOLUTION; MAXIMUM; OPTIMUM; MINIMUM; CYCLE; LENGTH; MAXIMUM; OPTIMUM; MINIMUM; PHASE; TIME
Derwent Class: T01; T07
International Patent Class (Main): **G06F-015/48**
File Segment: EPI

32/5/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

009628595 **Image available**
WPI Acc No: 1993-322144/199341
Related WPI Acc No: 1991-353378; 1991-369435; 1991-369436; 1991-369437; 1992-057025; 1992-160461; 1992-160462; 1992-323593; 1992-323650; 1992-331351; 1993-295576; 1993-328396; 1994-209005; 1994-225588; 1994-255598; 1996-077215; 1996-251377; 1997-192388
XRPX Acc No: N93-248245

Massively parallel processor **for image, multi-media and general purpose computing - has processing element unit** processor array **structure with single and dual processing elements, using finite difference method of solving differential equations**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DELGADO-FRIAS J G; PECHANEK G G; VASSILIADIS S; DELGADO-FNIAS J G
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 564847	A2	19931013	EP 93104154	A	19930315	199341	B
EP 564847	A3	19940720	EP 93104154	A	19930315	199528	
US 5577262	A	19961119	US 90526866	A	19900522	199701	
			US 91682786	A	19910408		
			US 91740266	A	19910805		
			US 91740355	A	19910805		
			US 91740556	A	19910805		
			US 91740568	A	19910805		
			US 92864112	A	19920406		
			US 94194653	A	19940209		
			US 95522163	A	19950713		
US 5612908	A	19970318	US 92864112	A	19920406	199717	
			US 94194364	A	19940209		
US 6405185	B1	20020611	US 92864112	A	19920406	200244	
			US 95551144	A	19950323		

Priority Applications (No Type Date): US 92864112 A 19920406; US 90526866 A 19900522; US 91682786 A 19910408; US 91740266 A 19910805; US 91740355 A 19910805; US 91740556 A 19910805; US 91740568 A 19910805; US 94194653 A 19940209; US 95522163 A 19950713; US 94194364 A 19940209; US 95551144 A

19950323
Cited Patents: No-SR.Pub; 5.Jnl.Ref; EP 456201; GB 2219106; US 4270170; US 4972361
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 564847	A2	E	37	G06F-015/80	
Designated States (Regional): DE FR GB					
EP 564847	A3			G06F-015/80	
US 5577262	A		31	G06F-015/00	CIP of application US 90526866
					CIP of application US 91682786
					CIP of application US 91740266
					CIP of application US 91740355
					CIP of application US 91740556
					CIP of application US 91740568
					Div ex application US 92864112
					Cont of application US 94194653
					CIP of patent US 5065339
					CIP of patent US 5146420
					CIP of patent US 5146543
					CIP of patent US 5148515
US 5612908	A		33	G06F-007/38	Div ex application US 92864112
US 6405185	B1			G06F-015/18	Cont of application US 92864112

Abstract (Basic): EP 564847 A

The apparatus includes a processing element unit **processor array** structure. The **processor array** structure includes single and dual processing elements that contain instruction and data storage units, receive instructions and data, and execute instructions.

The processing elements are interconnected by a processor interconnection apparatus. Further components support data initialisation, parallel function, wrap-around and broadcast processor communications.

USE/ADVANTAGE - Processor elements can improve image computing and improve speed. Apparatus can be used for multi-media and general purpose applications, including use of finite difference method of solving differential equations.

Dwg.3A/15

Title Terms: PARALLEL; PROCESSOR; IMAGE; MULTI; MEDIUM; GENERAL; PURPOSE; COMPUTATION; PROCESS; ELEMENT; UNIT; PROCESSOR; ARRAY; STRUCTURE; SINGLE; DUAL; PROCESS; ELEMENT; FINITE; DIFFER; METHOD; SOLVING; DIFFERENTIAL; EQUATE
Index Terms/Additional Words: MIMD; SIMD
Derwent Class: T01
International Patent Class (Main): **G06F-007/38 ; G06F-015/00 ; G06F-015/18 ; G06F-015/80**
File Segment: EPI

32/5/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

009116472 **Image available**
WPI Acc No: 1992-243909/199230
XRPX Acc No: N92-186127
Processor array **e.g. provided in computer system - has clocked buffers provided at each boundary between adjacent modules so as to provide communication link for buses**
Patent Assignee: SONY CORP (SONY)
Inventor: EASTTY P
Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2251964	A	19920722	GB 91852	A	19910115	199230	B
GB 2251964	B	19940914	GB 91852	A	19910115	199434	

Priority Applications (No Type Date): GB 91852 A 19910115

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2251964	A		24	G06F-013/40	
GB 2251964	B		2	G06F-013/40	

Abstract (Basic): GB 2251964 A

The array includes a number of processors (SP) arranged in modules or sub-arrays (A, B etc.). Each module includes a rectangular configuration of processors, preferably 4 x 4 interconnected by **vertical** and **horizontal** buses. Clocked buffers (R) are provided at each boundary between adjacent modules so as to provide a communication link for the corresponding buses. The **horizontal** and **vertical** processor interconnections are effectively split into a number of short buses.

A modularised implementation using processor and buffer cards may be used. The clocked buffers are **bidirectional** thus allowing communication to take place in either direction across each boundary.

ADVANTAGE - High operating speed can be maintained, and high signal bandwidth provided.

Dwg.1A/6

Title Terms: PROCESSOR; ARRAY; COMPUTER; SYSTEM; CLOCK; BUFFER; BOUNDARY; ADJACENT; MODULE; SO; COMMUNICATE; LINK; BUS

Derwent Class: T01

International Patent Class (Main): **G06F-013/40**

International Patent Class (Additional): **G06F-015/16**

File Segment: EPI

32/5/18 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

008882041 **Image available**

WPI Acc No: 1992-009310/199202

XRPX Acc No: N92-007155

Digital signal processing device for image processing - using linear array of one bit processing elements connected by shift registers and including serial parallel multipliers

Patent Assignee: CHEN K (CHEN-I); SVENSSON C M (SVEN-I); GENNUM CORP (GENN-N)

Inventor: CHEN K; SVENSSON C M

Number of Countries: 002 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 463721	A	19920102	EP 91303836	A	19910426	199202	B
CA 2040659	A	19911031				199204	
EP 463721	A3	19930616	EP 91303836	A	19910426	199405	
JP 6089271	A	19940329	JP 9199138	A	19910430	199417	
CA 2040659	C	19960507	CA 2040659	A	19910417	199628	

Priority Applications (No Type Date): CA 2040659 A 19910417; SE 901556 A 19900430

Cited Patents: NoSR.Pub; 4.Jnl.Ref; EP 293701

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

JP 6089271 A 17 G06F-015/16
CA 2040659 C H04N-005/38

Abstract (Basic): EP 463721 A

The video and image signal processing device (1) consists of a linear array of processing elements (**PE** 's) (2), external controller interface (4), I/O ports (6) to digitising cameras and display monitors, and an external memory interface (8). Single instruction multiple data (SIMD) topology is used incorporating two **modes** of communication, **horizontal** through shift registers (10,12) to other **PE** 's and vertically on a one bit bus within a **PE** .

There is one **PE** for each digital sample, or pixel, and the **PE** 's include a serial-parallel multiplier (16).

ADVANTAGE - Cost effective video image processing. (25pp Dwg.No.1/13

Title Terms: DIGITAL; SIGNAL; PROCESS; DEVICE; IMAGE; PROCESS; LINEAR; ARRAY; ONE; BIT; PROCESS; ELEMENT; CONNECT; SHIFT; REGISTER; SERIAL; PARALLEL; MULTIPLIER
Derwent Class: T01
International Patent Class (Main): **G06F-015/16** ; H04N-005/38
International Patent Class (Additional): **G06F-013/38** ; **G06F-015/80** ; G06T-001/00; H04N-005/14; H04N-007/13
File Segment: EPI

32/5/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

008736051 **Image available**
WPI Acc No: 1991-240067/199133
XRPX Acc No: N91-183087

Built-in self-test technique for read-only memories - by performing two polynomial divisions to provide residue in multiple input shift register which is examined for error

Patent Assignee: AT & T CORP (AMTT); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T BELL LAB (AMTT)
Inventor: ZORIAN Y
Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 441518	A	19910814	EP 91300663	A	19910129	199133	B
US 5091908	A	19920225	US 90475524	A	19900206	199211	
EP 441518	A3	19920701	EP 91300663	A	19910129	199333	
EP 441518	B1	19960904	EP 91300663	A	19910129	199640	
DE 69121733	E	19961010	DE 621733	A	19910129	199646	
			EP 91300663	A	19910129		
KR 180520	B1	19990415	KR 911618	A	19910131	200047	

Priority Applications (No Type Date): US 90475524 A 19900206
Cited Patents: NoSR.Pub; 4.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 441518	A				
Designated States (Regional): DE FR GB IT NL SE					
US 5091908	A		10		
EP 441518	B1	E	14	G11C-029/00	
Designated States (Regional): DE FR GB IT NL SE					
DE 69121733	E			G11C-029/00	Based on patent EP 441518
KR 180520	B1			G11C-029/00	

Abstract (Basic): EP 441518 A

The bits of a preselected quotient string are loaded into the n + 1 **column** of the memory. A polynomial division is performed on the entire contents of the memory by sequentially shifting out of the bits in the cells in each successive ROM **row** in a right-to-left direction into a separate one of the n + 1 inputs of a **bidirectional** multiple input shift register (18`). A second polynomial division is then performed by sequentially shifting the bits out of each successive **row** into the shift register (18`) in a left-to-right direction.

As each **row** of bits is shifted into the shift register during the second polynomial division, the register generates a quotient bit which is exclusively OR`d with a separate one of the quotient bits stored in the (n + 1) **column** of the memory, allowing for errors in the memory to be detected.

ADVANTAGE - Reduced error. (12pp Dwg.No.2/2

Title Terms: BUILD; SELF; TEST; TECHNIQUE; READ; MEMORY; PERFORMANCE; TWO; POLYNOMIAL; DIVIDE; RESIDUE; MULTIPLE; INPUT; SHIFT; REGISTER; ERROR

Derwent Class: U11; U13; U14

International Patent Class (Main): G11C-029/00

International Patent Class (Additional): **G06F-011/26**

File Segment: EPI

32/5/20 (Item 20 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

008646277 **Image available**

WPI Acc No: 1991-150306/199121

XRPX Acc No: N91-115416

Processor array **system with an SIMD architecture - has sub-array modules, each module having 32 processing elements, byte-wide arithmetic unit and multi-byte shift network**

Patent Assignee: AMT HOLDINGS LTD (AMTH-N)

Inventor: HUNT D

Number of Countries: 013 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 428327	A	19910522	EP 90312204	A	19901108	199121	B

Priority Applications (No Type Date): GB 8925721 A 19891114

Cited Patents: EP 191280; US 4144566

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 428327	A				

Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE

Abstract (Basic): EP 428327 A

The **processor array** system employing an SIMD architectures comprises a number of sub-arrays (S1...S4) modules. Each sub-array includes n=32 processing elements (**PE**). Each processing element is connected to a local store comprising on-chip memory; each chip is connected by an m-bit wide path (where m is greater than 1) to a block region of off-chip memory. The m-bit wide path is selectively configurable as one bit path to or from each of m processor elements, or as an m-bit wide path arranged to communicate complete m-bit words of memory data between the region of off-chip memory and respective processing elements.

Each processing element includes a byte-wide arithmetic unit (ALU) and byte-wide data paths for carrying data between the ALU and the on chip memory; each processing element further includes a four byte wide

32 bit operand shift network (Q) comprising a byte-wise shift network (Q1), and a bit-wise shift network (Q2) and an output register (Q0). Such **processor array** system is pref. connected to a host processor arranged to address the array as an extension of its own memory, via a scalar processor interface (MCU) for controlling the operation of the array.

USE/ADVANTAGE - Parallel processing computer systems, scan array system with SIMD architecture; significant improvement in performance of system when handling matrices, and corner turning can be carried out in transit between off-chip memory and the processing element using an n bit shift register, and arranging the off-chip memory in **horizontal mode** with a word length equal to number of processing elements. (Dwg.No.1/5)

Title Terms: PROCESSOR; ARRAY; SYSTEM; SIMD; ARCHITECTURE; SUB; ARRAY; MODULE; MODULE; PROCESS; ELEMENT; ARITHMETIC; UNIT; MULTI; BYTE; SHIFT; NETWORK

Derwent Class: T01

International Patent Class (Additional): **G06F-015/80**

File Segment: EPI

32/5/21 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

008607416 **Image available**

WPI Acc No: 1991-111446/199116

XRPX Acc No: N91-085967

Signal pipelining circuit for sync. vector processor - has input circuitry enabling pipelining of address data and control signals

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: BECKER M; CHILDERS J; CHUNG M; MIYAGUCHI H; REINECKE P; BECKER H; MOO T C

Number of Countries: 008 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 422963	A	19910417	EP 90311266	A	19901015	199116	B
EP 422963	A3	19930630	EP 90311266	A	19901015	199405	
US 5452425	A	19950919	US 89421494	A	19891013	199543	
			US 93163606	A	19931207		
EP 422963	B1	19970514	EP 90311266	A	19901015	199724	
US 5628025	A	19970506	US 89421471	A	19891013	199724	
			US 95483778	A	19950607		
DE 69030704	E	19970619	DE 630704	A	19901015	199730	
			EP 90311266	A	19901015		
US 5765010	A	19980609	US 89421471	A	19891013	199830	
KR 199073	B1	19990615	KR 9016355	A	19901013	200059	

Priority Applications (No Type Date): US 89421487 A 19891016; US 89421471 A 19891013; US 89421494 A 19891013; US 93163606 A 19931207; US 95483778 A 19950607

Cited Patents: 4.Jnl.Ref; EP 317218; US 3566366

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 422963	A				
Designated States (Regional): DE FR GB IT LI					
US 5452425	A		88	G06F-009/26	Cont of application US 89421494
EP 422963	B1	E	114	G06F-015/80	
Designated States (Regional): DE FR GB IT NL					
US 5628025	A		87	G06F-003/14	Cont of application US 89421471
DE 69030704	E			G06F-015/80	Based on patent EP 422963

US 5765010 A G06F-015/00
KR 199073 B1 G06F-015/80

Abstract (Basic): EP 422963 A
The SVP device has one bit processor elements controlled in common by a sequencer, a state machine to enable operation as a parallel processing device.Each processor element includes a set of input registers,two sets of register files,a ste of working registers ,an arithmetic logic unit including a one bit fulll adder subtractor and a ste of output registers .
In video applications each processor element operates on ine pixel of a horizontal scan line and is capable of real-time digital processing of video signals.Included within the SVP device id input circuitry enabling pipelining of address, datat and control signals.The circuitry includes latches and signal coding and decoding circuitry.
ADVANTAGE-HIghly parallel in operation.
Dwg.1/67
Title Terms: SIGNAL; PIPE; CIRCUIT; SYNCHRONOUS; VECTOR; PROCESSOR; INPUT; CIRCUIT; ENABLE; PIPE; ADDRESS; DATA; CONTROL; SIGNAL
Derwent Class: T01
International Patent Class (Main): **G06F-003/14** ; **G06F-009/26** ; **G06F-015/00** ; **G06F-015/80**
International Patent Class (Additional): **G06F-009/06** ; G06T-001/20
File Segment: EPI

32/5/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

008182044 **Image available**
WPI Acc No: 1990-069045/199010
XRPX Acc No: N90-052850
Parallel processor array **system for computer - includes array support with M-bit wide edge register connected via data path**
Patent Assignee: AMT HOLDINGS LTD (AMTH-N); CAMBRIDGE PARALLEL PROCESSING LTD (CAMB-N)
Inventor: HUNT D J
Number of Countries: 014 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 357342	A	19900307	EP 89308611	A	19890824	199010	B
US 5150290	A	19920922	US 89397709	A	19890823	199241	
EP 357342	B1	19960403	EP 89308611	A	19890824	199618	
DE 68926136	E	19960509	DE 626136	A	19890824	199624	
			EP 89308611	A	19890824		

Priority Applications (No Type Date): GB 8820237 A 19880825
Cited Patents: 1.Jnl.Ref; EP 234147; US 3858183; US 4593373
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 357342	A	E	9		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 5150290	A		9	G06F-015/80	
EP 357342	B1	E	10	G06F-015/80	
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
DE 68926136	E			G06F-015/80	Based on patent EP 357342

Abstract (Basic): EP 357342 A
The **processor array** system includes an n-bit scalar processor (2) and an m x m-bit **processor array** (1), m and n being integers,

with m greater than n. The system also includes an array support circuit (3) which is connected between the scalar processor (2) and the **processor array** (1) and communicates data between them. The system may include an n-bit wide data path linking n-bit scalar processor registers in the scalar processor to the array support circuit (3) together with an m-bit wide data path linking the array support (3) to the **processor array** (1).

The array support (3) includes a register interface arranged to interface the n-bit scalar processor registers to the **processor array** (1). The array support also includes an m-bit wide edge register (ME) which is connected to the **processor array** via the m-bit wide data path. The array may employ an SIMD architecture with each of a number of **single bit** processing elements having associated with it local store.

ADVANTAGE - Increased processing power.

Dwg.1/4

Title Terms: PARALLEL; PROCESSOR; ARRAY; SYSTEM; COMPUTER; ARRAY; SUPPORT; BIT; WIDE; EDGE; REGISTER; CONNECT; DATA; PATH
Derwent Class: T01
International Patent Class (Main): **G06F-015/80**
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

32/5/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

007734805 **Image available**
WPI Acc No: 1988-368737/198851
Communication protocol for public service trunking system - translating message protocol and format between site controller and land link and between land link and dispatch console
Patent Assignee: GENERAL ELECTRIC CO (GENE); ERICSSON GE MOBILE COMMUNICATIONS (TELF); GENERAL ELECTRIC CO LTD (ENGE); ERICSSON GE MOBILE COMMUNICATIONS INC (TELF); ERICSSON-GE MOBILE COMMUNICATIONS INC (TELF); ERICSSON INC (TELF)
Inventor: CHILDRESS J S; HUGHES H H; GORDON R T; HATTEY D L; NAZARENKO D M; YURMAN B; COOPER G M; DISSOSWAY M A; HALL N; SPANGLER F
Number of Countries: 006 Number of Patents: 060
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8809969	A	19881215	WO 88US1983	A	19880603	198851	B
GB 2206018	A	19881221	GB 8813168	A	19880603	198851	
GB 2206019	A	19881221	GB 8813016	A	19880603	198851	
GB 2206020	A	19881221	GB 8813167	A	19880603	198851	
JP 1004126	A	19890109	JP 88134560	A	19880602	198907	
JP 1004133	A	19890109				198907	
JP 64002435	A	19890106	JP 88135797	A	19880603	198907	
US 4821292	A	19890411	US 8756924	A	19870603	198917	
DK 8803054	A	19890315				198922	
US 4835731	A	19890530	US 8785572	A	19870814	198926	
DK 8803052	A	19890317				198928	
DK 8803053	A	19890317				198928	
DK 8900507	A	19890403				198929	
GB 2215946	A	19890927	GB 892033	A	19890131	198939	
US 4903262	A	19900220	US 8785490	A	19870814	199014	
US 4903321	A	19900220	US 8785663	A	19870814	199014	
US 4905234	A	19900227	US 8756923	A	19870603	199015	
US 4905302	A	19900227	US 8756922	A	19870603	199015	
JP 2500713	W	19900308	JP 88505629	A	19880603	199016	

US 4926496	A	19900515	US 8785491	A	19870814	199024	
CA 1282117	C	19910326				199117	
CA 1283455	C	19910423				199121	
US 5020132	A	19910528	US 89365810	A	19890306	199124	
GB 2206020	B	19910710				199128	
GB 2243273	A	19911023	GB 9110433	A	19910514	199143	
CA 1290401	C	19911008				199148	
GB 2244889	A	19911211	GB 9111268	A	19910524	199150	
GB 2244890	A	19911211	GB 9111269	A	19910524	199150	
CA 1292779	C	19911203				199204	N
GB 2215946	B	19920122				199204	
GB 2243273	B	19920122				199204	
US 5086506	A	19920204	US 89442319	A	19891128	199208	
GB 2247380	A	19920226	GB 9110869	A	19910520	199209	
CA 1295370	C	19920204				199212	
US 5109543	A	19920428	US 89449790	A	19891213	199220	
GB 2206018	B	19920603	GB 8813168	A	19880603	199223	
GB 2206019	B	19920603	GB 8813169	A	19880603	199223	
GB 2244889	B	19920603	GB 8813168	A	19880603	199223	
			GB 9111268	A	19910524		
GB 2244890	B	19920603	GB 8813168	A	19880603	199223	
			GB 9111269	A	19910524		
GB 2247380	B	19920603	GB 8813169	A	19880603	199223	
			GB 9110869	A	19910520		
US 5125102	A	19920623	US 8756922	A	19870603	199228	
			US 90464053	A	19900103		
US 5128930	A	19920707	US 8785572	A	19870814	199230	
			US 89365810	A	19890306		
			US 91666841	A	19910308		
CA 1304132	C	19920623	CA 566663	A	19880512	199231	
CA 1305524	C	19920721	CA 580065	A	19881013	199235	N
US 5175866	A	19921229	US 8757046	A	19870603	199303	
			US 90532164	A	19900605		
US 5206863	A	19930427	US 8785572	A	19870814	199318	
			US 89365810	A	19890306		
			US 91666862	A	19910308		
US 5212724	A	19930518	US 8785572	A	19870814	199321	
			US 89365810	A	19890306		
			US 91666860	A	19910308		
			US 92915769	A	19920721		
US 5265093	A	19931123	US 8785490	A	19870814	199348	
			US 89449790	A	19891213		
			US 92832697	A	19920207		
US 5274837	A	19931228	US 8756922	A	19870603	199401	
			US 90464053	A	19900103		
			US 92860159	A	19920330		
US 5274838	A	19931228	US 8757046	A	19870603	199401	
			US 90532164	A	19900605		
			US 92913906	A	19920716		
CA 1326510	C	19940125	CA 566664	A	19880512	199409	N
			CA 616065	A	19910509		
CA 1336920	C	19950905	CA 616065	A	19910509	199542	N
			CA 616659	A	19930610		
US 5483670	A	19960109	US 8756922	A	19870603	199608	
			US 90464053	A	19900103		
			US 92860159	A	19920330		
			US 93105153	A	19930812		
US 5574788	A	19961112	US 8756922	A	19870603	199651	
			US 90464053	A	19900103		
			US 92860159	A	19920330		
			US 93105153	A	19930812		

			US 95425152	A	19950419	
KR 9600153	B1	19960103	KR 88831	A	19880130	199905
US 5864762	A	19990126	US 8756922	A	19870603	199911
			US 90464053	A	19900103	
			US 92860159	A	19920330	
			US 93105153	A	19930812	
			US 95425152	A	19950419	
			US 96697330	A	19960822	
KR 9604810	B1	19960413	KR 88830	A	19880130	199914
KR 9609454	B1	19960719	KR 88832	A	19880130	199921
KR 9611123	B1	19960820	KR 882186	A	19880303	199924
JP 3019308	B2	20000313	JP 88128571	A	19880527	200017

Priority Applications (No Type Date): US 8785663 A 19870814; US 8756922 A 19870603; US 8756923 A 19870603; US 8756924 A 19870603; US 8757046 A 19870603; US 8785490 A 19870814; US 8785491 A 19870814; US 8785572 A 19870814; US 89365810 A 19890306; US 89442319 A 19891128; US 89449790 A 19891213; US 90464053 A 19900103; US 91666841 A 19910308; CA 580065 A 19881013; US 90532164 A 19900605; US 91666862 A 19910308; US 91666860 A 19910308; US 92915769 A 19920721; US 92832697 A 19920207; US 92860159 A 19920330; US 92913906 A 19920716; CA 616065 A 19910509; CA 616659 A 19930610; US 93105153 A 19930812; US 95425152 A 19950419; US 96697330 A 19960822

Cited Patents: US 4422171; US 4511958; US 4549297; US 4672601; US 4672655; US 4672658; US 4677656; US 4694473; US 4712214; US 4712229; US 4730348

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8809969	A	E	224		
Designated States (National): DK GB JP KR					
JP 3019308	B2		53	H04L-001/16	Previous Publ. patent JP 64002435
US 4821292	A		14		
US 4835731	A		118		
US 4903262	A		27		
US 4903321	A		63		
US 4905234	A		52		
US 4926496	A		15		
US 5086506	A		63		
US 5109543	A		24		
GB 2244889	B			H04Q-007/02	Derived from application GB 8813168
GB 2244890	B			H04Q-007/02	Derived from application GB 8813168
GB 2247380	B			H04B-007/14	Derived from application GB 8813169
US 5125102	A		37		Div ex application US 8756922
US 5128930	A		60	H04J-003/26	Div ex application US 8785572
					Div ex application US 89365810
					Div ex patent US 4835731
					Div ex patent US 5020132
US 5175866	A		39	H04B-001/74	Cont of application US 8757046
US 5206863	A		56	G06F-011/10	Div ex application US 8785572
					Div ex application US 89365810
					Div ex patent US 4835731
					Div ex patent US 5020132
US 5212724	A		60	H04M-011/00	Div ex application US 8785572
					Div ex application US 89365810
					Cont of application US 91666860
					Div ex patent US 4835731
					Div ex patent US 5020132
US 5265093	A		25	H04B-001/38	Div ex application US 8785490
					Div ex application US 89449790
					Div ex patent US 4903262
					Div ex patent US 5109543
US 5274837	A		34	H04B-007/14	Div ex application US 8756922

				Div ex application US 90464053
				Div ex patent US 4905302
				Div ex patent US 5125102
US 5274838	A	35	H04B-001/60	Cont of application US 8757046
				Cont of application US 90532164
				Cont of patent US 5175866
CA 1326510	C		H04B-007/24	Div ex application CA 566664
CA 1336920	C		H04B-007/15	Div ex application CA 616065
US 5483670	A	35	H04B-007/14	Div ex application US 8756922
				Div ex application US 90464053
				Div ex application US 92860159
				Div ex patent US 4905302
				Div ex patent US 5125102
				Div ex patent US 5274837
US 5574788	A	36	H04L-009/00	Div ex application US 8756922
				Div ex application US 90464053
				Div ex application US 92860159
				Div ex application US 93105153
				Div ex patent US 4905302
				Div ex patent US 5125102
				Div ex patent US 5274837
				Div ex patent US 5483670
US 5864762	A		H04Q-007/28	Div ex application US 8756922
				Div ex application US 90464053
				Div ex application US 92860159
				Div ex application US 93105153
				Div ex application US 95425152
				Div ex patent US 4905302
				Div ex patent US 5125102
				Div ex patent US 5274837
				Div ex patent US 5483670
				Div ex patent US 5574788
GB 2206018	B		H04Q-007/02	
GB 2206019	B		H04B-007/14	
CA 1304132	C		H04B-007/15	
CA 1305524	C		H04B-007/15	
KR 9600153	B1		H04L-001/16	
KR 9604810	B1		H04B-007/24	
KR 9609454	B1		H04B-007/00	
KR 9611123	B1		H04B-007/14	

Abstract (Basic): WO 8809969 A

The signal communication method comprises sending signals in a predetermined protocol between the site controller and a down link trunking card module over a **serial** data **link** . The digital signals are translated from one protocol to another. The signals in the second protocol are communicated between the down link trunking card module and a switch module remote from the site, over another **serial** data **link** .

The second protocol signals are translated into further protocol signals. These signals are communicated between the switch trunking card module and the processor.

USE - In trunk radio repeater system

Title Terms: COMMUNICATE; PROTOCOL; PUBLIC; SERVICE; TRUNK; SYSTEM; TRANSLATION; MESSAGE; PROTOCOL; FORMAT; SITE; CONTROL; LAND; LINK; LAND; LINK; DISPATCH; CONSOLE

Derwent Class: T01; W01; W02

International Patent Class (Main): **G06F-011/10** ; H04B-001/38; H04B-001/60; H04B-001/74; H04B-007/00; H04B-007/14; H04B-007/15; H04B-007/24; H04J-003/26; H04L-001/16; H04L-009/00; H04M-011/00; H04Q-007/02; H04Q-007/28

International Patent Class (Additional): G08C-025/00; G08C-025/02; H01J-007/04; H04B-001/02; H04B-001/40; H04B-003/36; H04B-007/204; H04B-007/26; H04B-017/02; H04J-003/22; H04L-011/20; H04L-012/56; H04M-003/22; H04Q-007/04; H04Q-009/02
File Segment: EPI

32/5/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

007713479 **Image available**
WPI Acc No: 1988-347411/198849
XRPX Acc No: N88-263313
Parallel data processing array data matrices - is divided into two groups each having processor units operating with associated single- column **multiple-** row **memory groups**
Patent Assignee: EATON CORP (EAYT); APPLIED INTELLIGENT SYSTEMS INC (INTE-N)
Inventor: WILSON S S
Number of Countries: 014 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 293700	A	19881207	EP 88108175	A	19880520	198849	B
US 5129092	A	19920707	US 8757128	A	19870601	199230	
EP 293700	B1	19950201	EP 88108175	A	19880520	199509	
DE 3852909	G	19950316	DE 3852909	A	19880520	199516	
			EP 88108175	A	19880520		

Priority Applications (No Type Date): US 8757128 A 19870601
Cited Patents: 5.Jnl.Ref; A3...8942; EP 150449; EP 6748; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 293700	A	E	24		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 5129092	A		22	G06F-015/80	
EP 293700	B1	E	28	G06F-015/76	
Designated States (Regional): DE FR GB NL					
DE 3852909	G			G06F-015/76	Based on patent EP 293700

Abstract (Basic): EP 293700 A

The parallel processing system (9) consists of an array of identical individual neighbourhood processing units and an associated array of **single - bit** -wide memories. The processor units are arranged in groups of eight (as 10a-10h) and similarly the memories are arranged in corresponding groups (as 13a-13h). The groups of eight processor units are linked by connections (11-21) for transferring data between the groups. Each group of memories constitutes eight one-bit **column** multiple - **row** memories.

One group of processor units is arranged for operating one parallel rows of data from the associated group of memories and for operating selectively in parallel on data from any one of the eight **columns** of the associated group of memories. A second group of processor units is arranged similarly for operating on data from its associated memories.

ADVANTAGE - Allows fixed array of processors to handle large array of data whilst performing operations requiring neighbourhood and global data processing

Title Terms: PARALLEL; DATA; PROCESS; ARRAY; DATA; MATRIX; DIVIDE; TWO; GROUP; PROCESSOR; UNIT; OPERATE; ASSOCIATE; SINGLE; **COLUMN** ; MULTIPLE; **ROW** ; MEMORY; GROUP

Derwent Class: T01
International Patent Class (Main): **G06F-015/76 ; G06F-015/80**
International Patent Class (Additional): **G06F-007/50 ; G06F-015/06 ; G06F-015/62** ; G06K-009/54
File Segment: EPI

32/5/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

007550645 **Image available**
WPI Acc No: 1988-184577/198827
XRPX Acc No: N88-141018
Computer system memory read-out apparatus - has serially - connected **registers shifting trigger signal with free-running clock signal to trigger address register**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: IBI T
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 273642	A	19880706	EP 87311070	A	19871216	198827	B
US 5033001	A	19910716	US 87134860	A	19871218	199131	
EP 273642	B1	19930407	EP 87311070	A	19871216	199314	
DE 3785324	G	19930513	DE 3785324	A	19871216	199320	
			EP 87311070	A	19871216		

Priority Applications (No Type Date): JP 86301621 A 19861219
Cited Patents: 1.Jnl.Ref; A3...9004; EP 161639; EP 242572; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 273642	A	E	12		
Designated States (Regional): DE FR GB					
EP 273642	B1	E	14	G11C-007/00	
Designated States (Regional): DE FR GB					
DE 3785324	G			G11C-007/00	Based on patent EP 273642

Abstract (Basic): EP 273642 A

The free-running clock signal (FCLK) is generated by the CPU and a gated clock signal is generated based on the free-running clock and on a stop signal. The stop signal is maintained at logic zero during a **normal** clock **mode** and at logic one for the single clock mode. In the single clock mode, the address register is switched at the instant of the appearance of the sixth clock signal (Tim 6) from the gated clock.

The first AND gate (A1) responds to the sixth clock signal and to the selection signal (SELO) from the decoder (DEC) to output the trigger signal (TRi) to the second AND gate (A2). Shift registers (SR1-3) shift the trigger signal in synchronism with the seventh and eight clock pulses of the free running clock to provide the read data clock signal (RCLK) to the read data register (RD-REG).

ADVANTAGE - Shortened read cycle period is achieved to enhance computer throughput.

4/7

Title Terms: COMPUTER; SYSTEM; MEMORY; READ; APPARATUS; SERIAL; CONNECT; REGISTER; SHIFT; TRIGGER; SIGNAL; FREE; RUN; CLOCK; SIGNAL; TRIGGER; ADDRESS; REGISTER
Derwent Class: T01; U14
International Patent Class (Main): G11C-007/00
International Patent Class (Additional): **G06F-001/04 ; G06F-005/06 ; G06F-013/00** ; G11C-008/00

File Segment: EPI

32/5/26 (Item 26 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

007311486
WPI Acc No: 1987-308493/198744
XRPX Acc No: N87-230768

Video attribute decoder for colour or monochrome display - has dot-broadening circuit and logic for doubling height of characters incorporating any number of segments

Patent Assignee: BULL SA (SELA)
Inventor: LECOURTIER G
Number of Countries: 007 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 244280	A	19871104	EP 87400711	A	19870401	198744 B
FR 2597691	A	19871023				198750
US 4831369	A	19890516	US 8741008	A	19870421	198923
EP 244280	B	19900627				199026
DE 3763466	G	19900802				199032
ES 2016632	B	19901116				199051

Priority Applications (No Type Date): FR 865682 A 19860421
Cited Patents: EP 84122; US 4479119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 244280	A	F	18		
	Designated States (Regional): DE ES GB IT NL				
US 4831369	A		16		
EP 244280	B				
	Designated States (Regional): DE ES GB IT NL				

Abstract (Basic): EP 244280 A

A clock circuit (25), a configuration register (23), a character attribute register (22) and a line attribute register (32,33) are connected to a decoding circuit (21). This feeds a character masking circuit (41) whose output is serialised (40) for a dot broadener (54) controlling the multiplexing (50) of background colour and inversion signals (52,53) and a character colour signal (51).

Double-height logic (31) operates on output of the line attribute register (32,33) to control the selection lines (LCO-LC3) of a set of characters in read-only memory where e.g. 9. x 10 dot matrix character representations are stored.

ADVANTAGE - With choice between 'professional' high-definition alphanumeric and videotex semigraphic **modes** , brightness differences between **vertical** and horizontal lines are avoided. Characters comprising any number of segments can be displayed with double height on any type of monitor.

Title Terms: VIDEO; ATTRIBUTE; DECODE; COLOUR; MONOCHROME; DISPLAY; DOT; BROADEN; CIRCUIT; LOGIC; DOUBLE; HEIGHT; CHARACTER; INCORPORATE; NUMBER; SEGMENT
Derwent Class: P85; T04
International Patent Class (Additional): **G06F-003/15** ; G09G-001/28; H04N-005/66
File Segment: EPI; EngPI

32/5/27 (Item 27 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

004756267
WPI Acc No: 1986-259608/198640
XRPX Acc No: N86-194081
Register providing built-in test facilities for integrated circuit - operates in at leas three modes **including** normal **input-output** mode , **shift mode and test mode**
Patent Assignee: INT COMPUTERS LTD (INCM)
Inventor: HALE S G; NAVEN F
Number of Countries: 009 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 196171	A	19861001	EP 86301545	A	19860305	198640	B
AU 8655021	A	19860925				198646	
JP 61223675	A	19861004	JP 8664284	A	19860324	198646	
ZA 8601856	A	19860918				198652	
US 4701916	A	19871020	US 86840602	A	19860317	198744	
EP 196171	B	19911116				199145	
DE 3682305	G	19911212				199151	

Priority Applications (No Type Date): GB 8518857 A 19850725; GB 857612 A 19850323
Cited Patents: 1.Jnl.Ref; A3...8905; EP 111053; EP 148403; GB 2085171; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 196171	A	E	16		
Designated States (Regional): DE FR GB IT NL					
EP 196171	B				
Designated States (Regional): DE FR GB IT NL					

Abstract (Basic): EP 196171 B
The register has a serial input (SDI) which is fed via two test control cells (T1,T2) and a multiplexer (12) to a series of eight **single bit** cells (D0 to D7). The parallel data inputs (PD0 to PD7) and outputs (D0 to D7) can be connected to the processing element of the integrated circuit. The output of an exclusive-OR gate tree (15), fed from the outputs of four of the cells, is fed back to the multiplexer (12). A control circuit (16) produces signals to control the mode switching functions.
In **normal** RUN **mode** , all ten cells (T1,T2,B0 to B7) operate as parallel input/output registers. In SHIFTS mode, the cells are looped from input to output, allowing test data to be shifted in or out as required. In TEST mode, the test cells (T1,T2) can set the register into states which enable it to act as a pseudo-random number generator, a test analyser or a digital signature analyser.
USE/ADVANTAGE - Several registers can be used in VLSI chip to provide rapid built-in test facilities. Number of extra input paths to the register required to select different modes of operations is reduced. (16pp Dwg.No.2/5
Title Terms: REGISTER; BUILD; TEST; FACILITY; INTEGRATE; CIRCUIT; OPERATE; LEA; THREE; MODE; NORMAL; INPUT; OUTPUT; MODE; SHIFT; MODE; TEST; MODE
Derwent Class: T01; U11; U13
International Patent Class (Additional): G01R-031/28; **G06F-011/26** ; G11C-019/00; G11C-029/00; H01L-021/66; H01L-027/06
File Segment: EPI

32/5/28 (Item 28 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

004117938
WPI Acc No: 1984-263479/198442
XRPX Acc No: N84-196970

Dynamic memory accessing controller - operates in data refresh, and refresh with error, correction and detection modes and has read write mode responding to CPU request

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: BRCICH J A; LEVY R J; MADEWELL J; THREEWITT N B
Number of Countries: 012 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8403968	A	19841011	WO 84US400	A	19840314	198442	B
EP 138964	A	19850502	EP 84901514	A	19840314	198518	
JP 60500979	W	19850627	JP 84501428	A	19840314	198532	
US 4542454	A	19850917	US 83480996	A	19830330	198540	
EP 138964	B	19900131				199005	
DE 3481236	G	19900308				199011	

Priority Applications (No Type Date): US 83480996 A 19830330
Cited Patents: 4.Jnl.Ref; US 4183096; US 4319356; US 4369510; US 4380812; US 4412314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8403968	A	E			
Designated States (National): JP					
Designated States (Regional): AT BE CH DE FR GB LI NL SE					
EP 138964	A	E			
Designated States (Regional): AT BE CH DE FR GB LI LU NL SE					
EP 138964	B	E			
Designated States (Regional): AT BE CH DE FR GB LI LU NL SE					

Abstract (Basic): WO 8403968 A

The controller controls access to a memory under four modes. The controller receives address data from a CPU and produces memory access address data. A timing controller controls the dynamic memory controller (DMC). A 2-bit mode control (MC) word with bits 06O(and!MCq!ar e!reci)

EP 138964 A

A controller for accessing a dynamic memory (14) having a plurality of banks (B0-B3), and a plurality of rows and a plurality of columns for each of the plurality of banks (B0-B3), the memory (14) storing data which are subject to being refreshed and to data bit errors, said controller having a read/write mode and a refresh mode and a refresh with error detection and correction mode, comprising: (a) a latch (56) for storing first address data for addressing the memory (14) for the read/write mode, the first address data having a first row address portion (52R), a first column address portion (52C) and a first bank address portion (52B), (b) means (44,38) for carrying a row address strobe input (RAS1), a column address strobe input (CAS1), a mode control input (54) identifying any one said mode and a multiplexer select input (MSEL); (c) an address counter (58) responsive to said mode control input (54) and said row address strobe input (RAS1) for generating second address data for addressing the memory (14) for the refresh mode and the refresh with error detection and correction mode, the second address data having a second row address portion, a second column address portion and a bank address portion, (d) multiplexer means (70), responsive to said mode control input (54) and said multiplexer select input (MSEL) for outputting to the memory (14) the

first row address portion and the first column address portion for the read/write **mode** or the second **row** address portion and the second column address portion for the refresh mode or the refresh with error detection and correction **mode** , (e) **row** address strobe decoder means (88) responsive to said first bank address portion (52B), said mode control input (54) and said row address strobe input (RAS1), for producing and outputting to the memory (14) any one of a

Title Terms: DYNAMIC; MEMORY; ACCESS; CONTROL; OPERATE; DATA; REFRESH; REFRESH; ERROR; CORRECT; DETECT; MODE; READ; WRITING; MODE; RESPOND; CPU; REQUEST

Derwent Class: T01

International Patent Class (Additional): **G06F-011/00** ; **G06F-012/16** ; G11C-007/00; G11C-011/34

File Segment: EPI

32/5/29 (Item 29 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2002 Thomson Derwent. All rts. reserv.

004045439

WPI Acc No: 1984-190981/198431

XRPX Acc No: N84-142726

Digital polarity correlator integrated circuit - implements mathematical functions using comparator, delaying shift register and counter

Patent Assignee: NAT RES DEV CORP (NATR)

Inventor: BLACKLEY W S; JACK M A; JORDON J R

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2133908	A	19840801	GB 8414	A	19840103	198431	B
GB 2133908	B	19860806	GB 8414	A	19840103	198632	
US 4602349	A	19860722	US 84569894	A	19840111	198632	

Priority Applications (No Type Date): GB 836797 A 19830311; GB 83699 A 19830119; GB 8414 A 19840103

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2133908	A		9		

Abstract (Basic): GB 2133908 A

A self-testing facility is provided in a correlator comprising a delaying shift register whose stages are respectively associated with a set of channels each incorporating a coincidence detector and an integrating counter. A further shift register is provided which is used to inspect for the overload condition of the counters, the normal running condition involving application of binary signals respectively to the delaying shift register and to all the coincidence detectors.

The operation of each channel is tested in a **mode** involving inhibition of **normal** running condition, and information indicative of faulty channels is recorded in a register. This information is used in the normal running condition to cause by-passing of those stages of the shift registers corresponding to faulty channels.

ADVANTAGE - Uses NMOS technology to achieve over 100 parallel stages of correlation on single chip.

0/5

Title Terms: DIGITAL; POLARITY; CORRELATE; INTEGRATE; CIRCUIT; IMPLEMENT; MATHEMATICAL; FUNCTION; COMPARATOR; DELAY; SHIFT; REGISTER; COUNTER

Derwent Class: T01

International Patent Class (Additional): **G06F-007/02** ; **G06F-011/20** ; **G06F-015/33**

File Segment: EPI

32/5/30 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2002 Thomson Derwent. All rts. reserv.

003609546
WPI Acc No: 1983-F7742K/198317
XRPX Acc No: N83-075336
Multi-dimensional data processing computer - simultaneously processes large number of parallel signals to enable high speed processing of parallel data arrays
Patent Assignee: NAT AERO & SPACE ADMIN (USAS)
Inventor: FROSCH R A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4380046	A	19830412				198317 B

Priority Applications (No Type Date): US 7941143 A 19790521
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4380046	A		15		

Abstract (Basic): US 4380046 A
The appts. processes multidimensional data with strong spatial characteristics, such as raw image data, characterized by a large number of parallel data streams in an ordered array. The appts. comprises a large number (e.g. 18,384 in a 128 x 128 array) of parallel processing elements operating simultaneously and independently on **single bit** slices of a corresp. array of incoming data streams under control of a single set of instructions.
Each of the processing elements comprises a **bidirectional** data bus in communication with a register for storing **single bit** slices together with a random access memory unit and associated circuitry, including a binary counter. The shift register device, for performing logical and arithmetical computations on the bit slices, and an I/O unit for interfacing the **bidirectional** data bus with the data stream source. The **massively parallel processor** architecture enables very high speed processing of large amounts of ordered, parallel data, including spatial translation by shifting or sliding of bits **vertically** or **horizontally** to neighbouring processing elements.
1/15
Title Terms: MULTI; DIMENSION; DATA; PROCESS; COMPUTER; SIMULTANEOUS; PROCESS; NUMBER; PARALLEL; SIGNAL; ENABLE; HIGH; SPEED; PROCESS; PARALLEL ; DATA; ARRAY
Derwent Class: T01; W02; W04
International Patent Class (Additional): **G06F-015/16**
File Segment: EPI

32/5/31 (Item 31 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

06562657 **Image available**
COORDINATE INPUT DEVICE ADAPTABLE TO USB SUSPEND MODE

PUB. NO.: 2000-148390 [JP 2000148390 A]
PUBLISHED: May 26, 2000 (20000526)

INVENTOR(s): WATANABE KAZUHIRO
APPLICANT(s): FUJITSU TAKAMISAWA COMPONENT LTD
APPL. NO.: 10-316419 [JP 98316419]
FILED: November 06, 1998 (19981106)
INTL CLASS: **G06F-003/033**

ABSTRACT

PROBLEM TO BE SOLVED: To provide a coordinate input device adaptable to a USB suspend mode that reduces the current consumption in the suspend mode and does not impair the responsiveness during the time in the suspend mode.

SOLUTION: Light emitting diodes 16 and 18 of X, Y axis encoders 21 and 22 are **serially connected** and are connected with a DC current source Vcc via a first current control circuit 24 and a second current control circuit 25. When a measured value of a counter in a control part 23 is changed, the coordinate input device is regarded as in a **normal mode** and the current is supplied to the light emitting diodes 16, 18 via the first current control circuit 24. When the measured value of the counter in the control part 23 is not changed, the coordinate input device is regarded as in the suspend mode and the current to be supplied to the light emitting diodes 16, 18 is reduced by the second current control circuit 25.

COPYRIGHT: (C)2000,JPO

32/5/32 (Item 32 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

06097663 **Image available**
TEST CIRCUIT

PUB. NO.: 11-039182 [JP 11039182 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): SHIRATA SHUICHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 09-188780 [JP 97188780]
FILED: July 14, 1997 (19970714)
INTL CLASS: **G06F-011/22** ; **G06F-011/22** ; G01R-031/28; H01L-027/04; H01L-021/822

ABSTRACT

PROBLEM TO BE SOLVED: To reduce an excess load to a burn in device by providing a pull up resistance changing means to short-circuit an interval between a first resistance and a test terminal when output potential of an inverter is at an L level, to shield the interval and to define a pull up resistance as flue first resistance, or the first and a second resistances at an H level.

SOLUTION: When a microcomputer is used at a **normal** operation **mode** , the potential of a gate terminal 6a of a P channel transistor 6 shows the L level. For this reason, the P channel transistor is turned on, a drain terminal 6b and a source terminal 6c are conducted and a resistance 5 and the test terminal 2 are short-circuited. As a result, the pull up resistance is defined as the resistance 5. When the microcomputer is used at a test mode, the potential of the gate terminal 6a of the P channel transistor 6 shows the H level. For this reason, the P channel transistor 6 is turned off and the drain terminal 6b and the source terminal 6c are shielded. As the result, the pull up resistance is defined as the resistance 5 + a resistance 7 since the resistance 5 and the resistance 7 are **serially connected** .

COPYRIGHT: (C)1999,JPO

32/5/33 (Item 33 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

04531977 **Image available**
FIFO BUFFER DIAGNOSTIC CIRCUIT

PUB. NO.: 06-175877 [JP 6175877 A]
PUBLISHED: June 24, 1994 (19940624)
INVENTOR(s): KIMURA ETSUZO
APPLICANT(s): NEC ENG LTD [329822] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-206375 [JP 92206375]
FILED: August 03, 1992 (19920803)
INTL CLASS: [5] **G06F-011/22**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1806, Vol. 18, No. 516, Pg. 31, September 28, 1994 (19940928)

ABSTRACT

PURPOSE: To easily diagnose a FIFO buffer formed inside an integrated circuit in a short time.

CONSTITUTION: At the time of a diagnostic mode, a diagnostic signal Sd is supplied to an input terminal 102. A mode setting signal Sm for setting the diagnostic **mode** or a **normal mode** is supplied to an input terminal 103. Input switching circuits 21-24 are provided on the input side of flip-flops 11-14 constituting a FIFO buffer 10. When the mode setting signal Sm shows the diagnostic mode, the input switching circuits 21-24 select the diagnostic signal Sd and when the **normal mode** is shown, the flip-flops 11-14 are **serially connected** . An AND circuit 30 ANDs output signals S1-S4 from the respective flip-flops 11-14 and outputs the result as a signal Sa. An OR circuit 40 ORs output signals from the flip-flops 11-14 and outputs the result as a signal Sb. An arithmetic result switching circuit 50 selects either of the signals Sa and Sb corresponding to the diagnostic signal Sd.

32/5/34 (Item 34 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

03930853 **Image available**
PARALLEL DATA PROCESSOR WITH BUILT-IN TWO-DIMENSIONAL ARRAY OF ELEMENT PROCESSOR AND SUB-ARRAY UNIT OF ELEMENT PROCESSOR

PUB. NO.: 04-295953 [JP 4295953 A]
PUBLISHED: October 20, 1992 (19921020)
INVENTOR(s): KONDO TOSHIO
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-082968 [JP 9182968]
FILED: March 25, 1991 (19910325)
INTL CLASS: [5] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1496, Vol. 17, No. 107, Pg. 51, March

04, 1993 (19930304)

ABSTRACT

PURPOSE: To improve the transfer capacity and to execute the 90 degree rotation at a high speed by providing an inter-adjacent element processor transfer line of one bit width, and a transfer line of plural bit width connected in a double-level between the left end and the right end of a row, in the **column** direction and the row direction, respectively, in a matrix consisting of element processors.

CONSTITUTION: A **processor array** part 3 consisting of element processors (**PE**) 10 is connected to a data bus through **bidirectional** buffers 8, 9. In the **column** direction of the **PE** 10, an inter-adjacent **PE** transfer line of one bit width is provided. In the **row** direction of the **PE** 10, a transfer line of plural bit width connected in a double- level between the left end and the right end of the **row** is provided. By the double-level connection, and enlargement of bit width of the transfer line in the **row** direction, the transfer capacity in the **row** direction in a one-dimensional operation mode is improved. Also, one-dimensional array data can directly be delivered to the outside of the **processor array** part 3. Also, the data can be delivered between a transfer system in the **row** direction and a transfer system in the **column** direction, and the 90 degree rotation is easily executed.

32/5/35 (Item 35 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

03923559 **Image available**
PROCESSOR ARRAY

PUB. NO.: 04-288659 [JP 4288659 A]
PUBLISHED: October 13, 1992 (19921013)
INVENTOR(s): PIITAA IISUTEI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-005598 [JP 925598]
FILED: January 16, 1992 (19920116)
PRIORITY: 9100852 [GB 91852], GB (United Kingdom), January 15, 1991 (19910115)
INTL CLASS: [5] **G06F-015/16** ; **G06F-013/38** ; **G06F-013/40**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1492, Vol. 17, No. 90, Pg. 67, February 23, 1993 (19930223)

ABSTRACT

PURPOSE: To easily extend a **processor array** without reducing the processing speed by providing plural processor modules and buffers connecting adjacent modules.

CONSTITUTION: Processors SP in each of processor modules A, B, E, and F are arranged in a matrix of 4X4. Processors SP in each module communicate with one another through **vertical** busses VB and **horizontal** busses HB. Busses VB and HB receive supply of a clock signal at regular intervals synchronously with one another. **Bidirectional** clock buffers R are provided on boundaries of adjacent modules and connect corresponding busses of adjacent modules. Modules communicate with one another through buffers R controlled by the clock. Though modules are added to extend the **processor**

array , the processing speed of each module is not reduced because length of busses in modules is fixed.

32/5/36 (Item 36 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

02580320 **Image available**
NORMALIZING CIRCUIT

PUB. NO.: 63-197220 [JP 63197220 A]
PUBLISHED: August 16, 1988 (19880816)
INVENTOR(s): UEDA KATSUHIKO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-030317 [JP 8730317]
FILED: February 12, 1987 (19870212)
INTL CLASS: [4] **G06F-007/00**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 801, Vol. 12, No. 480, Pg. 162, December 15, 1988 (19881215)

ABSTRACT

PURPOSE: To avoid such a case where the normalizing result is equal to -2(sup n) by performing the left shift by an extent equal to the value obtained by subtracting '1' from the output of a 1st means when the output of a 2nd means is equal to '1'.
CONSTITUTION: A shifter control circuit A11 outputs the control outputs L(sub 0), L(sub 1) and L(sub 2) to a table 1 (not shown here) with the output of a register 10 defined as an input based on the input/output relation. A shifter control circuit B12 outputs the control output R based on the input/output relation shown in a table 2 (not shown here). Then a left 1-bit shifter 14 controlled by the output L(sub 0) is added together with a left 2-bit shifter 15 controlled by the output L(sub 1), a left 4-bit shifter 16 controlled by the output L(sub 2), and a right 1-bit shifter 13 controlled by the output R. The data shown in a table 2 is shifted left by an extent equal to the value subtracting a **single bit** and therefore can be normalized in an equivalent way as the shift **mode** of a conventional **normalizing** circuit in a state where a negative number is expressed in a compliment of '2'. It is not needed to use a subtractor that calculates a left shift number reduced by a **single bit** . Thus, a normalizing action is performed at a high speed.

32/5/37 (Item 37 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

02546679 **Image available**
GRAPHIC BOUNDARY VECTOR GENERATING CIRCUIT

PUB. NO.: 63-163579 [JP 63163579 A]
PUBLISHED: July 07, 1988 (19880707)
INVENTOR(s): FUJIOKA YOICHI
APPLICANT(s): SEIKO INSTR & ELECTRONICS LTD [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-314960 [JP 86314960]
FILED: December 25, 1986 (19861225)
INTL CLASS: [4] **G06F-015/66**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)

JOURNAL: Section: P, Section No. 786, Vol. 12, No. 431, Pg. 68, November 15, 1988 (19881115)

ABSTRACT

PURPOSE: To attain high speed processing by successively reading the picture elements of a two-dimensional picture memory in which a graphic picture whose contour is being extracted is stored in an X direction or a Y direction and sequentially storing a start point and end point address on which the picture elements are present on a memory capable of reading from a main computer in a pipeline mode.

CONSTITUTION: An address generating circuit indicated for a picture element unit is added, a series of the start point and end point addresses of the picture elements having a **straight line** continuity in **horizontal** and **vertical** directions are detected by the use of a simple circuit constituted of address counters 4, 5, a -1 circuit 7 and a coincidence detector 8 or the like and **successively connected** to a start point and end point address storing memory 9 in the pipeline mode. Namely, when an operation command is issued from the main computer, this circuit generates a picture element address at high speed, detects the start point and end point addresses of the successive picture elements and successively stores in the memory capable of reading from the main computer. Thereby, the main computer may process only the data in the start point and the end point address storing memory 9 when the operation of this circuit is completed.

32/5/38 (Item 38 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

02324121 **Image available**

INFORMATION INPUT DEVICE

PUB. NO.: 62-241021 [JP 62241021 A]
PUBLISHED: October 21, 1987 (19871021)
INVENTOR(s): MIYAGISHIMA TAKAO
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-082387 [JP 8682387]
FILED: April 11, 1986 (19860411)
INTL CLASS: [4] **G06F-003/033 ; G06F-003/03**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 687, Vol. 12, No. 112, Pg. 79, April 09, 1988 (19880409)

ABSTRACT

PURPOSE: To avoid such a case where an information input device is unavailable as a whole by reediting again the contents to be displayed on a display screen if a touch sensor has a defective element.

CONSTITUTION: When a initial action instruction is delivered, a control part 8 of a touch sensor decides the defective state of an element. The defect of a **single bit** or so is neglected and a rise is given to a system. If it is impossible to neglect the defect area, the commands are given to a main control part 6 from the part 8 and a control part 10 to reedit the display contents of a display screen 9. For instance, the displays are switched between an input part and an operation explaining part or the position of the input part is shifted to avoid the coincidence between the input part and the defect area. In case such a reediting action is impossible, an information input device has an error. While the present screen is registered as it is when the input part is not coincident with

the defect area. Thus it is possible to perform the self-diagnosis to detect the position of a defective element through comparison with the screen of a **normal mode** .

32/5/39 (Item 39 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

01866318 **Image available**
SELF-CHECK CIRCUIT OF TRANSPARENT ELECTRODE TOUCH PANEL

PUB. NO.: 61-080418 [JP 61080418 A]
PUBLISHED: April 24, 1986 (19860424)
INVENTOR(s): YAMADA MITSUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-201682 [JP 84201682]
FILED: September 28, 1984 (19840928)
INTL CLASS: [4] **G06F-003/03**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 492, Vol. 10, No. 254, Pg. 65, August 30, 1986 (19860830)

ABSTRACT
PURPOSE: To improve the reliability of the titled check circuit by connecting an optional resistance to X and Y electrodes respectively and applying a signal of -V to an electrode at the side of a drive circuit from a self-check control circuit to actuate a receiving circuit and to detect the disconnection of a transparent electrode.

CONSTITUTION: In a self-check mode, a current flows to Y electrodes 51-54 from a control circuit 10 via a drive circuit 2 and resistances 71-77 for self- check circuits. Then a receiving circuit 3 is actuated. The voltage -V which flows a current is applied for **sequential connections** secured among X electrodes 61-64 and Y electrodes 51-54 respectively. Then the circuit 3 for electrodes 61-64 is actuated to check the disconnection of those electrodes 51-54 and 61-64. The current flows to the resistances 71-77 even in a **normal** operation **mode** . This current, however, is very small and therefore the circuit 3 is not actuated to produce no problem. Then the switching is possible between the normal operation and self-check modes by a control switch circuit 11 which is actuated by a signal (a).

32/5/40 (Item 40 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

00985964 **Image available**
SINGLE ERROR CORRECTING AND DOUBLE ERROR DETECTING CIRCUIT

PUB. NO.: 57-136264 [JP 57136264 A]
PUBLISHED: August 23, 1982 (19820823)
INVENTOR(s): HIRAOKA TAKASHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-021487 [JP 8121487]
FILED: February 18, 1981 (19810218)
INTL CLASS: [3] **G06F-011/10** ; G11C-029/00
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)

JOURNAL: Section: P, Section No. 157, Vol. 06, No. 237, Pg. 92, November 25, 1982 (19821125)

ABSTRACT

PURPOSE: To inform the information of the occurrence of a **single bit** error to the outside when necessary by means of the signal which decides whether or not the above-mentioned information should be informed to the outside.

CONSTITUTION: In case the information on a single error is required for an inspection of a main storage, a set signal is transmitted and set to an S-R type flip flop circuit 33 from a CPU. As a result, an AND gate 34 is capable of delivering an output, and the single error information to be fed to an error correcting circuit 32 is trnamitted to the CPU from a readout information inspecting circuit 31 via an AND gate 34 and an OR gate 35. On the other hand, the circuit 33 is reset in the **normal** operation **mode** . As a result, the gate 34 is incapable of delivering an output, and the error information is not sent to the CPU but processed within a single error correcting and double error detecting circuit.

32/5/41 (Item 41 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2002 JPO & JAPIO. All rts. reserv.

00571957 **Image available**

ADDITIONAL PROCESSOR

PUB. NO.: 55-059557 [JP 55059557 A]
PUBLISHED: May 06, 1980 (19800506)
INVENTOR(s): AKIYOSHI TOSHIHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 53-132185 [JP 78132185]
FILED: October 27, 1978 (19781027)
INTL CLASS: [3] **G06F-011/00** ; **G06F-003/00**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 19, Vol. 04, No. 100, Pg. 162, July 18, 1980 (19800718)

ABSTRACT

PURPOSE: To realize a direct fault diagnosis for the additional processor based on the soft ware order by dividing the actions of the central processor and the additional processor into the **normal mode** and the test mode and then switching the both modes via the software order.

CONSTITUTION: When the order is drawn out of memory device 3 by CPU1 and decoded as the **normal mode** , **mode** switch holding circuit 10 is set to the **normal mode** . And at the same time, the **normal mode** information plus the additional processor action start information are transferred to additional processor 2. These information are then given to control circuit 22 to execute and process the additional **processor order** to device 3. In the test mode, circuit 10 is set to the test mode, and at the same time the test information is transferred to processor 2. This test information is stored in mode switch holding circuit 20, and then the diagnosis is given to each part of the additional processor in the test mode.

Search report

Set	Items	Description
S1	49195	MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCESSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGEMENT? OR ORDER OR FORMATION)
S2	24995	(SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N)(CONNECT? OR LINK?) OR SINGLE()BIT
S3	4365	MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?)
S4	16290	MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5	1303	MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6	467	VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7	469376	VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8	718794	HORIZONTAL? OR ROW OR NORMAL?
S9	248409	BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE
S10	0	S1 (S) S2 (S) S3 (S) S4 (S) S5 (S) S6
S11	111	S1 (S) S2
S12	0	S3 (S) S4 (S) S5 (S) S6
S13	9	S3 (S) S4 (S) S5
S14	10	S1 (S) S6
S15	7	S2 (S) S6
S16	7	S11 (S) S3
S17	10	S11 (S) S4
S18	3	S11 (S) S5
S19	0	S11 (S) S6
S20	36	S13 OR S14 OR S15 OR S16 OR S17 OR S18
S21	23	S20 AND IC=G06F?
S22	72960	S1 OR S2
S23	113	S22 (S) S7 (S) S8 (S) S9
S24	25	S23 AND IC=G06F?
S25	21	S24 NOT S20
S26	44	S21 OR S25
S27	44	IDPAT (sorted in duplicate/non-duplicate order)
S28	44	IDPAT (primary/non-duplicate records only)

File 348:EUROPEAN PATENTS 1978-2002/Jul W03
(c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020725,UT=20020718
(c) 2002 WIPO/Univentio

28/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

01134339
Document image processing apparatus for processing line portions manually input to document image, method therefor, and computer readable recording medium recorded with document image processing program therefor
Apparat und Verfahren zum Verarbeiten von Dokumentbildern fur das Nachbearbeiten von per Hand in das Dokumentbild eingegeben Linien und computerlesbares Speichermedium mit darauf gespeicherten Bearbeitungsprogramm
Appareil et methode de traitement d'images de documents pour retoucher des lignes entrees a la main dans l'image de document et medium d'enregistrement lisible par ordinateur avec le programme enregistre
PATENT ASSIGNEE:
Sharp Kabushiki Kaisha, (2795030), 22-22, Nagaike-cho Abeno-ku, Osaka-shi Osaka, (JP), (Applicant designated States: all)
INVENTOR:
Kanemoto, Yuko, 192-15, Mikasa, Tawaramoto-cho, Shiki-gun, Nara, (JP)
Hirosawa, Masashi, 212 Raporu Senzai, 266-1, Sugimoto-cho, Tenri-shi, Nara, (JP)
Yamanoue, Masafumi, 3-28-302, Kujohirano-cho, Yamatokoriyama-shi, Nara, (JP)
LEGAL REPRESENTATIVE:
MULLER & HOFFMANN Patentanwalte (101521), Innere Wiener Strasse 17, 81667 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 990994 A2 000405 (Basic)
APPLICATION (CC, No, Date): EP 99119466 990930;
PRIORITY (CC, No, Date): JP 98279226 981001
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/24** ; **G06F-017/21**

ABSTRACT EP 990994 A2
A document image processing apparatus has the following construction in order to draw a manually input line portion along a desired character string in a document image in good style and high operability. More specifically, the image data (36D) of a document read by a scanner (1A) is displayed at a display portion (2). At this time, when the user operates a tablet (3A) to manually draw a line portion (L) along a desired character string in the displayed document (S2), a row region (LE1) along which the manually input line portion is drawn is extracted from the region of the document image by a row extracting portion (4) based on positional information represented by the input data (36A) of the manually drawn line portion and the document image data. The manually drawn line portion is corrected into a straight line along the extracted row region for display by curve correcting portion (5).
ABSTRACT WORD COUNT: 154
NOTE:
Figure number on first page: 1A

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 20000405 A2 Published application without search report
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 200014 1174
SPEC A (English) 200014 11209

Total word count - document A 12383
Total word count - document B 0
Total word count - documents A + B 12383

INTERNATIONAL PATENT CLASS: **G06F-017/24** ...

... **G06F-017/21**
...SPECIFICATION Y-direction is taken, a character region CE1 for each character is finally detected (see Fig. 7F).
Row region extracting portion 9 extracts a **row** region based on the direction of the input data 36A of free curve L for image data 36D in processing region **PE** . As an example of the method of extracting a **row** region, projections XSD and YSD of each character region CE1 in the X- and Y- directions may be used. According to this method, a projection is taken in the direction **perpendicular** to the direction of input data 36A for information on each character region CE1, a **row** region (or a **column** region) can be extracted. More specifically, let us now assume that information on a plurality of character...

...in the X-direction, when a projection YSD in the Y-direction is taken (see Fig. 8B), **row** region LE1 may be extracted (see Fig. 8C). **Row** region LE1 may be extracted without using such information of the plurality of character regions CE1. If...

...in the X-direction in Fig. 7D, information on both ends is cut out, at least one **row** region LE1 is extracted.
Each of the extracted row regions LE1 is defined by rectangular region data...

28/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00996862
Start code detecting apparatus for video data stream
Vorrichtung zur Startkodedetektierung fur Videodatenstrom
Appareil de detection de code de depart pour un flux de donnees video
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Applicant designated States: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, WickLane Stinchcombe, Dursley, Gloucestershire G11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-under-edge, Gloucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 901287 A2 990310 (Basic)
EP 901287 A3 990922
APPLICATION (CC, No, Date): EP 98202166 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)

INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; **G06F-009/38**

ABSTRACT EP 901287 A2
A system having a plurality of processing stages, comprising a universal adaptation unit in the form of an interactive interfacing token for control and/or data functions among said processing stages,

wherein said token is a CODING(underscore)STANDARD token for conditioning said system for processing in a selected one of a plurality of picture compression/ decompression standards; one of said processing stages being a Huffman decoder and parser; one of said control tokens being a CODING(underscore)STANDARD control token; and upon receipt of said CODING(underscore)STANDARD control token, said parser is reset to an address location corresponding to the location of a program for handling the picture standard identified by said CODING(underscore)STANDARD control token.
ABSTRACT WORD COUNT: 112
NOTE:
Figure number on first page: 61

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	990310 A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	990310 A2	Date of filing of request for examination: 980629
Search Report:	990922 A3	Separate publication of the search report

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9910	191
SPEC A	(English)	9910	126718
Total word count - document A			126909
Total word count - document B			0
Total word count - documents A + B			126909

...INTERNATIONAL PATENT CLASS: **G06F-013/00** ...

... **G06F-009/38**

...SPECIFICATION systems which do not use control tokens.
The control tokens are generated by circuitry within the decoder **processor** and emulate the operation of a number of different type standard-dependent signals passing into the serial...480, 30 Hz, 4:2:0
. Flexible chroma sampling formats
. Full JPEG baseline decoding
. Glue-less page **mode** DRAM interface
. 208 pin PQFP package
. Independent coded data and decoder clocks
. Re-orders MPEG picture sequence...word of Token supplied (coded(underscore)extn goes low).
3)First byte of data supplied in byte **mode** . A new DATA Token is automatically created on-chip.

A.10.2 Supplying data via the MPI...non-data Tokens.

A.12.10 Counter flushed too early
If a FLUSH token arrives at the **bit** counter before the bit count target is attained, an event is generated which can cause an interrupt...

...between the output of the Huffman decoder and the input of the spatial video decoding circuits (inverse **modeler** , quantizer and DCT). This

second logical buffer allows processing time to include a spread so as to ...

28/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00996861
Multistandard decoder for Huffman codes
Mehrnormendekodierer fur Huffmancodes
Decodeur multistandard de codes de Huffman
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IE;IT;LI;NL)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchhay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Riddin gs, Wick Lane Stinchcombe, Dursley, GLoucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Sprin ghill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley,Coombe, Wotton-Under-Edge, Gloucester GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 901286 A1 990310 (Basic)
APPLICATION (CC, No, Date): EP 98202135 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00 ; G06F-009/38**

ABSTRACT EP 901286 A1
A Huffman decoder for decoding data words encoded according to the Huffman coding provisions of either H.261 or MPEG standards, the data words including an identifier that identifies the Huffman code standard under which the data words were coded, comprising :
means for receiving the Huffman coded data words, including means for reading the identifier to determine which standard governed the Huffman coding of the received data words, and means for converting the data words to JPEG Huffman coded data words, if necessary, in response to reading the identifier that identifies the Huffman coded data words as H.261 or MPEG Huffman coded ;

means, operably connected to the Huffman coded data words receiving means, for generating an index number associated with each JPEG Huffman coded data word receiving an index number from the index number generating means, and including an output that is a decoded data word corresponding to the index number.
ABSTRACT WORD COUNT: 155

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 990310 A1 Published application (A1with Search Report ;A2without Search Report)
Examination: 990310 A1 Date of filing of request for examination: 980626

Examination: 990901 A1 Date of dispatch of the first examination report: 19990713
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9910	390
SPEC A	(English)	9910	126718
Total word count - document A			127108
Total word count - document B			0
Total word count - documents A + B			127108

...INTERNATIONAL PATENT CLASS: **G06F-013/00** ...
... **G06F-009/38**

...SPECIFICATION systems which do not use control tokens.
The control tokens are generated by circuitry within the decoder **processor** and emulate the operation of a number of different type standard-dependent signals passing into the serial...480, 30 Hz, 4:2:0
. Flexible chroma sampling formats
. Full JPEG baseline decoding
. Glue-less page **mode** DRAM interface
. 208 pin PQFP package
. Independent coded data and decoder clocks
. Re-orders MPEG picture sequence...word of Token supplied (coded(underscore)extn goes low).
3)First byte of data supplied in byte **mode** . A new DATA Token is automatically created on-chip.

A.10.2 Supplying data via the MPI...non-data Tokens.

A.12.10 Counter flushed too early
If a FLUSH token arrives at the **bit** counter before the bit count target is attained, an event is generated which can cause an interrupt...
...between the output of the Huffman decoder and the input of the spatial video decoding circuits (inverse **modeler** , quantizer and DCT). This second logical buffer allows processing time to include a spread so as to ...

28/5,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucesterhire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:

Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00 ; G06F-009/38**
CITED PATENTS (EP B): EP 572766 A; EP 576749 A; WO 94/25935 A
CITED REFERENCES (EP B):
MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, page 294/295 XP000427624 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT" ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, no. CONF. 17, 15 August 1988, pages 209-216, XP000079309
YONG M CHONG: "A DATA-FLOW ARCHITECTURE FOR DIGITAL IMAGE PROCESSING" WESCON CONFERENCE RECORD,1 January 1984, pages 4/6 1-4/6 10, XP000565437
KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, February 1988, pages 111-117, XP000051576;

ABSTRACT EP 884910 A1

A pipeline system having an inverse modeller stage and an inverse discrete cosine transform stage, comprising a processing stage, positioned between said inverse modeller stage and said inverse discrete cosine transform stage, responsive to tokens for processing data, wherein said tokens each comprise a plurality of data words, each said word including an extension indicator which indicates a presence or an absence of additional words in said token, a length of said token being determined by said extension indicators, whereby the length of said token can be unlimited;

wherein said tokens are communicated from said inverse modeller stage to said processing stage.

ABSTRACT WORD COUNT: 104

NOTE:
Figure number on first page: 76

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	000607	A1	International Patent Classification changed: 20000419
Application:	981216	A1	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020502	B1	No opposition filed: 20020212
Lapse:	020403	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509,
Grant:	010509	B1	Granted patent
Change:	000607	A1	Title of invention (French) changed: 20000419
Change:	000607	A1	Title of invention (English) changed: 20000419
Change:	000607	A1	Title of invention (German) changed: 20000419
Change:	000712	A1	International Patent Classification changed: 20000524
Change:	000712	A1	Title of invention (German) changed: 20000524

Change:	000712 A1	Title of invention (English) changed: 20000524
Change:	000712 A1	Title of invention (French) changed: 20000524
Lapse:	020320 B1	Date of lapse of European Patent in a contracting state (Country, date): BE 20010509,
Lapse:	020410 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509, CH 20010509, LI 20010509,
Examination:	981216 A1	Date of filing of request for examination: 980626
Examination:	990901 A1	Date of dispatch of the first examination report: 19990713

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739
Total word count - document A			127222
Total word count - document B			123759
Total word count - documents A + B			250981

...INTERNATIONAL PATENT CLASS: **G06F-013/00** ...

... **G06F-009/38**
...SPECIFICATION in the bit(underscore)count(underscore)target register. A target met event is then generated and the **bit** counter resets to zero and waits for the next FLUSH Token.
The bit counter will also stop...be generated for any subsequent bytes of extra(underscore)information(underscore)picture. If there is only a **single** byte of extra(underscore)information(underscore)picture, no Parser event will occur.

A.14.8 Changes at...

...The MPEG sequence header describes the following characteristic of the video about to be decoded:
(horizontal and **vertical** size
(pixel aspect ratio
(picture rate
(coded data rate
(...

28/5,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00893346
Semiconductor memory device
Halbleiterspeicheranordnung
Dispositif de memoire a semi-conducteurs
PATENT ASSIGNEE:
MITSUBISHI DENKI KABUSHIKI KAISHA, (208581), 2-3, Marunouchi 2-chome Chiyoda-ku, Tokyo, (JP), (Proprietor designated states: all)
MITSUBISHI ELECTRIC ENGINEERING CO., LTD., (1515570), 6-2 Ohte-machi 2-chome, Chiyoda-ku, Tokyo, (JP), (Proprietor designated states: all)

INVENTOR:
Dosaka, Katsumi, c/o Mitsubishi Denki K.K. LSI, Kenkyusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Kumanoya, Masaki, c/o Mitsubishi Denki K.K. LSI, Kenkyusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Yamazaki, Akira, c/o Mitsubishi Denki K.K. LSI, Kenkyusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Iwamoto, Hisashi, c/o Mitsubishi Denki K.K. LSI, Kenkyusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Konishi, Yasuhiro, c/o Mitsubishi Denki K.K. LSI, Kenkyusho, 1 Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Hayano, Kouji, c/o Mitsubishi Denki K.K., Kitaitami Seisakusho 1, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Abe, Hideaki, c/o Mitsubishi Denki K.K., Kitaitami Seisakusho 1, Mizuhara 4-chome, Itami-shi, Hyogo-ken, (JP)
Himukashi, Katsumitsu, Mitsubishi El. Eng. Co. Ltd, LSI Engineering Office, 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
Ishizuka, Yasuhiro, Mitsubishi El. Eng. Co. Ltd, LSI Engineering Office, 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
Saiki, Tsukasa, Mitsubishi El. Eng. Co. Ltd, LSI Engineering Office, 61-5 Higashino 4-chome, Itami-shi, Hyogo-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. High Holborn 2-5 Warwick Court, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 817198 A1 980107 (Basic)
EP 817198 B1 000315
APPLICATION (CC, No, Date): EP 97201598 920416;
PRIORITY (CC, No, Date): JP 9185625 910418; JP 91212140 910823; JP 91242286 910924; JP 9217809 920203
DESIGNATED STATES: DE; FR; GB; IT
RELATED PARENT NUMBER(S) - PN (AN):
EP 509811 (EP 92303424)
INTERNATIONAL PATENT CLASS: G11C-011/00; G11C-007/00; G11C-008/00; G11C-008/04; G11C-011/406; G11C-011/419; G11C-005/06; **G06F-012/08**
CITED PATENTS (EP B): EP 115187 A; EP 136819 A; EP 156316 A; EP 277763 A; EP 326953 A; EP 344752 A; EP 420339 A; DE 2329527 A; FR 2606199 A; US 4660180 A; US 4802129 A; US 4809156 A; US 4912630 A; US 4943960 A; US 4953131 A; US 4970418 A; US 4977538 A; US 4984206 A
CITED REFERENCES (EP B):
PATENT ABSTRACTS OF JAPAN vol. 11, no. 223, 21 July 1987 & JP 62 038590 A (FUJITSU)
PATENT ABSTRACTS OF JAPAN vol. 13, no. 198, 15 March 1989 & JP 63 285795 A (AGENCY OF IND SCIENCE & TECHOLOGY)
PATENT ABSTRACTS OF JAPAN vol. 14, no. 289, 21 June 1990 & JP 02 087392 A (HITACHI)
ARIMOTO ET AL: "a circuit design of intelligent cache dram with automatic write back capability." IEEE JOURNAL OF SOLID STATE CIRCUITS, vol. 26, no. 4, April 1991, NEW YORK US, pages 560-565, XP002043297
AMITAI ET AL: "BURST MODE MEMORIES IMPROVE CACHE DESIGN" IRE WESCON CONVENTION RECORD, October 1990, pages 29-33, XP002043298
PATENT ABSTRACTS OF JAPAN vol. 13, no. 375, 21 August 1989 & JP 01 128294 A (SHARP)
PATENT ABSTRACTS OF JAPAN vol. 11, no. 26, 24 January 1987 & JP 61 196345 A (NEC CORP)
PATENT ABSTRACTS OF JAPAN vol. 11, no. 58, 21 February 1987 & JP 61 222091 A (FUJITSU)
YAMADA ET AL: "A 64 KBIT MOS DYNAMIC RAM WITH AUTO/SELF REFRESH FUNCTIONS" ELECTRONICS AND COMMUNICATIONS INJAPAN, vol. 66, no. 1, January 1983, SILVER SPRING,MARYLAND,USA, pages 103-110, XP002043299
KUNG ET AL: "AN 8KX8 DYNAMIC RAM WITH SELF REFRESH" IEEE JOURNAL OF SOLID STATE CIRCUITS, vol. 17, no. 5, October 1982, NEW YORK,USA, pages

863-871, XP002043300
HAIDAKA ET AL : "THE CACHE DRAM ARCHITECTURE: A DRAM WITH AN ON-CHIP CACHE MEMORY" IEEE MICRO, vol. 10, no. 2, April 1991, NEW YORK,USA, pages 14-25, XP002043301;

ABSTRACT EP 817198 A1
A semiconductor memory device includes a DRAM (100), an SRAM (200) and a bi-direction transfer gate circuit (210) provided between SRAM (200) and DRAM (100). SRAM array (201; 560) includes a plurality of sets of word lines. Each set is provided in each row of SRAM array and each word line in each set is connected to a different group of memory cells of an associated row. An address signal for the SRAM and an address signal for the DRAM are separately applied to an address buffer (255). The semiconductor memory device further includes an additional function control circuit (229) for realizing a burst mode and a sleep mode. A data transfer path from DRAM to the SRAM and a data transfer path from the SRAM to the DRAM are separately provided in the bi-directional transfer gate circuit. Data writing paths (GIL) and (LIL) and data reading paths (LOL) and (GOL) are separately provided in the DRAM array. By the above described structure, operation of the buffer circuit is stopped in the sleep mode, reducing power consumption. Since data writing path and data reading path are separately provided in the DRAM array, addresses to the DRAM array can be applied in non-multiplexed manner, so that data can be transferred at high speed from the DRAM array to the SRAM array, enabling high speed operation even at a cache miss.
ABSTRACT WORD COUNT: 230
NOTE:
Figure number on first page: 9

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None:	010228 B1	No opposition filed: 20001216
Grant:	20000315 B1	Granted patent
Application:	980107 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	980304 A1	Date of filing of request for examination: 971224
Examination:	980520 A1	Date of despatch of first examination report: 980401

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199802	5803
CLAIMS B	(English)	200011	2935
CLAIMS B	(German)	200011	2533
CLAIMS B	(French)	200011	3808
SPEC A	(English)	199802	90313
SPEC B	(English)	200011	73947
Total word count - document A			96130
Total word count - document B			83223
Total word count - documents A + B			179353

...INTERNATIONAL PATENT CLASS: **G06F-012/08**

...SPECIFICATION of signal waveforms showing data transfer operation from the DRAM array to the SRAM array when the **bi - directional** data transfer circuit shown in Fig. 44 is employed.
Figs. 48A through 48F show, as an example...bus 251, and for detecting and amplifying information of the selected SRAM cells in data reading. A **bi - directional** transfer gate circuit 210 is provided between DRAM 100 and SRAM 200. Referring to Fig. 32, the...

28/5,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00711606
Start code detector for image sequences
Detektor fur den Startcode von Bildsequenzen
Detecteur de code de depart pour sequences d'images
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester. GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674443 A2 950927 (Basic)
EP 674443 A3 951213
EP 674443 A3 981223
EP 674443 B1 010509
APPLICATION (CC, No, Date): EP 95301301 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 891089 (EP 98202149)
(EP 98202154)
EP 884910 (EP 98202132)
EP 891088 (EP 98202133)
EP 897244 (EP 98202134)
EP 901286 (EP 98202135)
EP 901287 (EP 98202166)
EP 896473 (EP 98202170)
EP 896474 (EP 98202171)
EP 896476 (EP 98202174)
EP 896475 (EP 98202172)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00 ; G06F-009/38**
CITED PATENTS (EP B): EP 288219 A; EP 460751 A; EP 506294 A; EP 551672 A; EP 572263 A; EP 572766 A; EP 576749 A; EP 577329 A; EP 602621 A; WO 94/25935 A; GB 2269070 A; US 4622585 A; US 4823201 A; US 5173695 A; US 5253053 A
CITED REFERENCES (EP B):
KUN-MIN YANG ET AL: "VLSI ARCHITECTURE DESIGN OF A VERSATILE VARIABLE LENGTH DECODING CHIP FOR REAL-TIME VIDEO CODECS" PROCEEDINGS OF THE REGION 10 CONFERENCE ON COMPUTER AND COMMUNICATI SYSTEMS (TENCON), HONG KONG, 24 - 27 SEPT., 1990, vol. 2, 24 September 1990, pages 551-554, XP000235934 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, February 1988, pages 111-117, XP000051576
KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT" ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, 15 August 1988, pages 209-216,

XP000079309 BRIGGS F A
TOKUMICHI MURAKAMI ET AL: "A DSP ARCHITECTURAL DESIGN FOR LOW BIT-RATE MOTION VIDEO CODEC" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 36, no. 10, 1 October 1989, pages 1267-1274, XP000085313
ELLIOTT J A ET AL: "REAL-TIME SIMULATION OF VIDEOPHONE IMAGE CODING ALGORITHMS ON RECONFIGURABLE MULTICOMPUTERS" IEE PROCEEDINGS E. COMPUTERS & DIGITAL TECHNIQUES, vol. 139, no. 3 PART E, 1 May 1992, pages 269-279, XP000306411
MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, page 294/295 XP000427624 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
YONG M CHONG: "A DATA-FLOW ARCHITECTURE FOR DIGITAL IMAGE PROCESSING" WESCON CONFERENCE RECORD,1 January 1984, pages 4/6 1-4/6 10, XP000565437;

ABSTRACT EP 674443 A2
A multi-standard video decompression apparatus has a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned in certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token.
ABSTRACT WORD COUNT: 102
NOTE:
Figure number on first page: 61

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	010509	B1	Granted patent
Application:	950927	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020502	B1	No opposition filed: 20020212
Lapse:	020403	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509,
Lapse:	020320	B1	Date of lapse of European Patent in a contracting state (Country, date): BE 20010509,
Lapse:	020410	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509, CH 20010509, LI 20010509,
Search Report:	951213	A3	Separate publication of the European or International search report
*Search Report:	960110	A2	Separate publication of European or Intl search report (change)
Change:	971022	A2	Representative (change)
Change:	980304	A2	Obligatory supplementary classification (change)
Examination:	981104	A2	Date of filing of request for examination: 980908
Search Report:	981223	A3	Separate publication of the European or International search report
Examination:	990324	A2	Date of despatch of first examination report: 990208

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2897
CLAIMS B	(English)	200119	647
CLAIMS B	(German)	200119	609
CLAIMS B	(French)	200119	752
SPEC A	(English)	EPAB95	128616
SPEC B	(English)	200119	122384
Total word count - document A			131543
Total word count - document B			124392
Total word count - documents A + B			255935

...INTERNATIONAL PATENT CLASS: **G06F-013/00** ...
... **G06F-009/38**

...SPECIFICATION with the data. In this way, the identifier field acts as an instruction for the data-flow **processor** . The system directs each token to a specific data-flow processor using a module number (MN). If...

...SPECIFICATION halves to illustrate that each stage in this embodiment of the pipeline includes primary and secondary data **storage** elements. In Fig. 2, the primary data storage is shown as the right half of each stage
...2:0
(Flexible chroma sampling formats
(Can re-order the MPEG picture sequence
(Glue-less DRAM interface
(**Single** +5V supply
(208 pin PQFP package
(Max. power dissipation 2.5W
(Uses standard page mode DRAM
The...

28/5,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00711605
Reconfigurable data processing stage
Rekonfigurierbare Datenverarbeitungsstufe
Etage d'operation de donnees reconfigurable
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol, BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire, GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire, GL11 5PE, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674446 A2 950927 (Basic)
EP 674446 A3 960814
EP 674446 B1 010801
APPLICATION (CC, No, Date): EP 95301300 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; **G06F-009/38**

CITED PATENTS (EP B): EP 572766 A; EP 576749 A; WO 94/25935 A
CITED REFERENCES (EP B):
ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, 15 August 1988, BRIGGS F A, pages 209-216, XP000079309 KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT"

IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, pages 111-117, XP000051576 KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS"

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 36, no. 10, 1 October 1989, pages 1267-1274, XP000085313 TOKUMICHI MURAKAMI ET AL: "A DSP ARCHITECTURAL DESIGN FOR LOW BIT-RATE MOTION VIDEO CODEC"

IEE PROCEEDINGS E. COMPUTERS & DIGITAL TECHNIQUES, vol. 139, no. 3 PART E, 1 May 1992, pages 269-279, XP000306411 ELLIOTT J A ET AL: "REAL-TIME SIMULATION OF VIDEOPHONE IMAGE CODING ALGORITHMS ON RECONFIGURABLE MULTICOMPUTERS"

PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, page 294/295 XP000427624 MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION"

4TH INTERNATIONAL CONFERENCE ON SIGNAL PROCESSING APPLICATIONS & TECHNOLOGY, vol. 2, 28 September 1993 - 1 October 1993, SANTA CLARA, CALIFORNIA, US, pages 1031-1038, XP002014370 TOM KOPET: "Programmable architectures for real-time video compression"

WESCON '84 CONFERENCE RECORD, ANAHEIM, CA, USA, 30 October 1984 - 1 November 1984, pages 4.6.1-4.6.10, XP002014371 Y.M.CHONG: "A Data-Flow Architecure for Digital Image Processing";

ABSTRACT EP 674446 A3

A multi-standard video decompression apparatus has a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned in certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token. A wide variety of unique supporting subsystem circuitry and processing techniques are disclosed for implementing the system. (see image in original document)

ABSTRACT WORD COUNT: 144
NOTE:
Figure number on first page: 10

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	010801	B1	Granted patent
Application:	950927	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020724	B1	No opposition filed: 20020503
Lapse:	020410	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010801,
Lapse:	020717	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010801, BE 20010801,
Change:	960501	A2	International patent classification (change)
Change:	960501	A2	Obligatory supplementary classification (change)
Search Report:	960814	A3	Separate publication of the European or

International search report
Examination: 970409 A2 Date of filing of request for examination: 970212
Change: 971105 A2 Representative (change)
Examination: 990901 A2 Date of dispatch of the first examination report: 19990713
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2475
CLAIMS B	(English)	200131	1079
CLAIMS B	(German)	200131	1072
CLAIMS B	(French)	200131	1186
SPEC A	(English)	EPAB95	125236
SPEC B	(English)	200131	121335
Total word count - document A			127738
Total word count - document B			124672
Total word count - documents A + B			252410

...INTERNATIONAL PATENT CLASS: **G06F-013/00** ...

... **G06F-009/38**

...SPECIFICATION accept new data. Since Stage F is not able to transfer the data D1 in its primary **storage** elements downstream (the ACCEPT signal into Stage F is LOW) in Cycle 3, Stage E must, therefore...

28/5,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00664899
Dynamically reconfigurable interprocessor communication network for SIMD multi-processors and apparatus implementing same.
Dynamisches rekonfigurbares Prozessorkommunikationsnetzwerk fur SIMD-Multiprozessoren und Vorrichtung zu seinem Betrieb.
Reseau de communication entre processeurs a reconfiguration dynamique pour des multiprocesseurs de type SIMD et appareil pour sa mise en oeuvre.
PATENT ASSIGNEE:
Hughes Aircraft Company, (214913), 7200 Hughes Terrace P.O. Box 45066, Los Angeles, California 90045-0066, (US), (applicant designated states: BE;DE;ES;FR;GB;IT;NL;SE)
INVENTOR:
Shams, Soheil, 1706 Clark Lane, Nr. B, Redondo Beach, CA 90278, (US)
Shu, David B., 8748 Hanna Avenue, Canoga Park, CA 91304, (US)
LEGAL REPRESENTATIVE:
Witte, Alexander, Dr.-Ing. et al (46523), Witte, Weller, Gahlert & Otten Patentanwalte Rotebuhlstrasse 121, D-70178 Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 638867 A2 950215 (Basic)
EP 638867 A3 951018
APPLICATION (CC, No, Date): EP 94112550 940811;
PRIORITY (CC, No, Date): US 106465 930812
DESIGNATED STATES: BE; DE; ES; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-015/16**

ABSTRACT EP 638867 A2
In a SIMD architecture having a two-dimensional array of processing elements (10), where a controller broadcasts instructions to all processing elements (10) in the array, a dynamically reconfigurable switching means (14) useful to connect four of the processing elements

(10) in the array into a group in accordance with either the broadcast instruction of the controller or a special communication instruction held in one processing element (10) of the group is provided. The switch (14) includes at least one data line (54) connected to each processing element (10) in the group. A multiplexer is connected to each data line (54) and to the controller and to a configuration register. It is adapted to load the special communication instruction from the one processing element (10) in the group into a configuration register and to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines (54) as a source of data and applying the data therefrom to a source output port. A demultiplexer is connected to each data line (54) and to the controller and to said configuration register, and to the source output port of the multiplexer means, and adapted to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines (54) as a source of data and applying the data therefrom to a selected data line (54). The switch (14) also acts to connect processing elements (10) that cross chip partitions forming the processor array. Up to four such switches (14) can be used to connect a group of four processing elements (10). (see image in original document)

ABSTRACT WORD COUNT: 292

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	950215 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	951018 A3	Separate publication of the European or International search report
Withdrawal:	970122 A2	Date on which the European patent application was deemed to be withdrawn: 960419

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	1236
SPEC A	(English)	EPABF2	4502
Total word count - document A			5738
Total word count - document B			0
Total word count - documents A + B			5738

INTERNATIONAL PATENT CLASS: **G06F-015/16**

...SPECIFICATION partitioned among multiple chips. An example partition of this switch is shown in Figure 8. A single **bidirectional** wire per bus bit is used to connect neighboring PEs in the west side to corresponding neighbors in the east side. In addition to r.c. coordinates within a chip, each **PE** is identified by its chip number. For example, **PE** C3...

...1.n represents **PE** located on **row** 1 and **column** n in chip 3. Similarly, **PE** C3...

...out and **PE** C3...

...in represent output channel and input channel respectively, of this **PE** . Since the switch shown is controlled by **PE** C3...

28/5,K/9 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

(c) 2002 European Patent Office. All rts. reserv.

00638303

A data processing system and method thereof.
Datenverarbeitungssystem- und methode.
Systeme et methode de traitement des donnees.

PATENT ASSIGNEE:
MOTOROLA, INC., (205770), 1303 East Algonquin Road, Schaumburg, IL 60196, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Gallup, Michael G., 1102 Radam Circle, Austin, Texas 78745, (US)
Goke, L. Rodney, 5105 Dusty Trail Cove, Austin, Texas 78749, (US)
Seaton, Robert W. Jr., 4836 Trail Crest Circle, Austin, Texas 78735, (US)
Lawell, Terry G., 11522 Heathrow, Austin, Texas 78759, (US)
Osborn, Stephen G., 3816 South Lamar No. 2412, Austin, Texas 78704, (US)
Tomazin, Thomas J., 3703 Cookstown Drive, Austin, Texas 78759, (US)
LEGAL REPRESENTATIVE:
Spaulding, Sarah Jane et al (73531), Motorola, European Intellectual Property Operations, Jays Close, Viables, Basingstoke, Hants. RG22 4PD, (GB)
PATENT (CC, No, Kind, Date): EP 619557 A2 941012 (Basic)
EP 619557 A3 960612
APPLICATION (CC, No, Date): EP 94104274 940318;
PRIORITY (CC, No, Date): US 40779 930331
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-015/76 ; G06F-015/80 ; G06F-015/16 ; G06F-015/78 ; G06F-009/38 ; G06F-007/544 ; G06F-009/32 ; G06F-009/315**

ABSTRACT EP 619557 A2

A data processing system (55) and method thereof includes one or more data processors (10). Data processor (10) is capable of performing both vector operations and scalar operations. Using a single microsequencer (22), data processor (10) is capable of executing both vector instructions and scalar instructions. Data processor (10) also has a memory circuit (14) capable of storing both vector operands and scalar operands. (see image in original document)

ABSTRACT WORD COUNT: 82

LEGAL STATUS (Type, Pub Date, Kind, Text):

Refusal:	000816	A2	Date European patent application was refused: 20000406
Application:	941012	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	951102	A2	Obligatory supplementary classification (change)
Change:	960605	A2	Obligatory supplementary classification (change)
Search Report:	960612	A3	Separate publication of the European or International search report
Examination:	970212	A2	Date of filing of request for examination: 961212
Examination:	990127	A2	Date of despatch of first examination report: 981211
Change:	990922	A2	International Patent Classification changed: 19990802
Change:	990929	A2	Title of invention (German) changed: 19990809

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	5610
SPEC A	(English)	EPABF2	83930
Total word count - document A			89540
Total word count - document B			0

Total word count - documents A + B 89540

INTERNATIONAL PATENT CLASS: **G06F-015/76** ...
... **G06F-015/80** ...

... **G06F-015/16** ...

... **G06F-015/78** ...

... **G06F-009/38** ...

... **G06F-007/544** ...

... **G06F-009/32** ...

... **G06F-009/315**

...SPECIFICATION These signals transfer address or data information dependent on the Run/Stop mode of operation. In Run **mode** , this **bi - directional** port drives as an output in response to the write north microcode instruction (writen, vwriten), and serves...

...also bi-directional. If the OP signal indicates a Random Access transfer, and this device is selected (/ **ROW** and /COL are both asserted), this port will receive the LSB of the Random Access Address, and...

28/5,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00480045
Built-in self-test technique for read-only memories
Technik zum eingebauten Selbsttest fur Nur-Lese-Speicher
Technique pour auto-test integre pour memoires mortes
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Zorian, Yervant, 31B Chicopee Drive, Princetown, New Jersey 08540, (US)
LEGAL REPRESENTATIVE:
Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 441518 A2 910814 (Basic)
EP 441518 A3 920701
EP 441518 B1 960904
APPLICATION (CC, No, Date): EP 91300663 910129;
PRIORITY (CC, No, Date): US 475524 900206
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: G11C-029/00; **G06F-011/26**
CITED REFERENCES (EP A):
INTERNATIONAL TEST CONFERENCE, Sept 10-14, 1990 Washington, USA, Y. ZORIAN, A. IVANOV: "EEODM: An Effective BIST Scheme for ROMs", pages 871-879
THE TRANSACTIONS OF THE INSTITUTE OF ELECTRONICS, INFORMATION & COMMUNICATION ENGINEERS vol. E71, no. 10, October 1988, TOKYO, JAPAN pages 1013 - 1022; E. FUJIWARA: 'Referenceless Signature Testing using Bi-Directional LFSR'
JOURNAL OF ELECTRONIC TESTING: THEORY AND APPLICATIONS vol. 1, February 1990, pages 59 - 71; Y. ZORIAN, V. K. AGARWAL: 'Optimizing Error

Masking in BIST by Output Data Modification'
IEEE TRANSACTION ON COMPUTERS vol. 37, no. 9, September 1988, NEW YORK, USA pages 1142 - 1145; W. H. MCANNEY, J. SAVIR: 'Built-In Checking of the Correct Self-Test Signature';

ABSTRACT EP 441518 A2
Self-testing of a read only memory (10') containing an m x n+1 array of **single - bit** storage cells (12') is accomplished by first loading the bits of a preselected quotient string into the n+1 **column** of the memory. Thereafter, a first polynomial division is performed on the entire contents of the memory by sequentially shifting out of the bits in the cells in each successive ROM **row** in a right-to-left direction into a separate one of the n+1 inputs of a **bidirectional** multiple input shift register (18'). A second polynomial division is then performed on the m x n contents of the memory (10') by sequentially shifting the bits out of each successive **row** into the shift register (18') in a left-to-right direction. As each **row** of bits is shifted into the shift register (18') during the second polynomial division, the register generates a quotient bit which is exclusively OR'd with a separate one of the quotient bits stored in the n+1(sup(th) **column** of the memory, allowing for errors in the memory to be detected. At the conclusion of the second polynomial division, there remains in the register a residue, also indicative of the errors in the memory. (see image in original document)
ABSTRACT WORD COUNT: 205

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	910814	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	920701	A3	Separate publication of the European or International search report
Examination:	930203	A2	Date of filing of request for examination: 921207
Change:	940223	A2	Representative (change)
*Assignee:	940622	A2	Applicant (name, address) (change)
Examination:	941207	A2	Date of despatch of first examination report: 941024
Grant:	960904	B1	Granted patent
Oppn None:	970827	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1240
CLAIMS B	(English)	EPAB96	1259
CLAIMS B	(German)	EPAB96	1321
CLAIMS B	(French)	EPAB96	1442
SPEC A	(English)	EPABF1	5826
SPEC B	(English)	EPAB96	5904
Total word count - document A			7066
Total word count - document B			9926
Total word count - documents A + B			16992

...INTERNATIONAL PATENT CLASS: **G06F-011/26**

...ABSTRACT A2
Self-testing of a read only memory (10') containing an m x n+1 array of **single - bit** storage cells (12') is accomplished by first loading the bits of a preselected quotient string into the n+1 **column** of the memory. Thereafter, a first polynomial division is performed on the entire contents of the memory by sequentially shifting out of the bits in the cells in each successive ROM **row** in a right-to-left direction into

a separate one of the n+1 inputs of a **bidirectional** multiple input shift register (18'). A second polynomial division is then performed on the m x n contents of the memory (10') by sequentially shifting the bits out of each successive **row** into the shift register (18') in a left-to-right direction. As each **row** of bits is shifted into the shift register (18') during the second polynomial division, the register generates...

...OR'd with a separate one of the quotient bits stored in the n+1(sup(th) **column** of the memory, allowing for errors in the memory to be detected. At the conclusion of the...

...CLAIMS a read-only memory (ROM) (10) configured of an m row by n+1 column array of **single - bit** storage cells (12), where m and n are integers, the n+1(sup(th) **column** containing a separate one of a set of predetermined bits, CHARACTERIZED BY the steps of:

performing a...

...n+1 bits stored in the ROM by sequentially shifting the n+1 bits in each successive **row** in a first direction into a separate one of the inputs of an **bidirectional** multiple input shift register (18') (MISR) initialized with a predetermined seed;

performing a second polynomial division on...

...rows of the ROM by sequentially shifting each of the first n bits in each successive ROM **row** in a second, **opposite direction** into a separate one of the inputs of the MISR such that at the completion of the...

...generating a quotient bit in the MISR as each of the first n bits in each successive **row** of the ROM are shifted in the second direction into a separate one of the inputs of...

...the MISR with a separate one of the predetermined bits stored in the n+1(sup(th) **column** of the ROM;

detecting if a bit of a preselected state results when each separate bit in the n+1(sup(th) **column** of the ROM is logically combined with each separate quotient bit generated by the MISR, and if...

...for self-testing a ROM (10) containing an m row by n+1 column matrix array of **single bit** storage cells (12), the n+1(sup(th) **column** of the ROM containing a predetermined quotient string, the apparatus CHARACTERIZED BY:

counter means (16') for addressing a sequential one of the storage locations in each **row** of the ROM to cause the bits stored in each **row** to be sequentially shifted out in a separate one of two **opposite directions** ; and

bidirectional multiple input shift register (MISR) means (18') for: (a) performing a first polynomial division on the bits...

...m x n array of ROM storage cells as the bits in each of the first n **columns** of each **row** are shifted into the MISR mean and generating a residue following such division; (c) for producing a quotient bit as each of the n bits in each successive **row** are shifted into the MISR during the second polynomial division; (d) logically combining each successive quotient bit with a separate one of the bits stored in the n+1(sup(th) **column** of the ROM; and (e) detecting whether each bit resulting the logical combination of the produced quotient

...CLAIMS hereinafter referred to as ROM, being configured of an m row by n+1 column array of **single bit** storage cells (12), where m and n

are integers, and having a bidirectional multiple input shift register (18), hereinafter referred to as **bidirectional** MISR, having n+1 inputs and being initialised with a predetermined seed, CHARACTERISED BY
the n+1...

...Apparatus for self-testing a ROM (10) including an m row by n+1 column array of **single bit** storage cells (12), and a **bidirectional** multiple input shifter register (18), the apparatus CHARACTERISED BY:
the n+1(sup(th) column of the...

28/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00390104
System and method for transforming and filtering a video image.
System und Verfahren zum Umformen und Filtern von Videobildern.
Systeme et methode pour transformer et filtrer une image video.
PATENT ASSIGNEE:
AMPEX SYSTEMS CORPORATION, (1591830), 401 Broadway M-S 3-35, Redwood City, California 94063-3199, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Beaulier, Daniel A., 324 Yale Road, Menlo Park, California, (US)
Marsh, Theodore A., 5400 Fulton, San Fransisco, California, (US)
LEGAL REPRESENTATIVE:
Horton, Andrew Robert Grant et al (32021), BOWLES HORTON Felden House Dower Mews High Street, Berkhamsted Hertfordshire HP4 2BL, (GB)
PATENT (CC, No, Kind, Date): EP 378253 A2 900718 (Basic)
EP 378253 A3 900912
EP 378253 B1 940608
APPLICATION (CC, No, Date): EP 90105501 840330;
PRIORITY (CC, No, Date): US 483424 830408
DESIGNATED STATES: DE; FR; GB
RELATED PARENT NUMBER(S) - PN (AN):
EP 125003 (EP 843022088)
INTERNATIONAL PATENT CLASS: H03H-017/02; **G06F-015/68 ; G06F-015/62**
CITED PATENTS (EP A): EP 52847 A; EP 52847 A; US 4328426 A
CITED REFERENCES (EP A):
RCA REVIEW, vol. 42, no. 1, March 1981, pages 3-59; G.A. REITMEIER: "Spatial compression and expansion of digital television images"
IDEM
IEEE TRANSACTIONS ON COMPUTER, vol. C-31, no. 10, October 1982, pages 934-942, IEEE, New York, US; M.R. WARPENBURG et al.: "SIMD image resampling"
XEROX DISCLOSURE JOURNAL, vol. 5, no. 1, January/February 1980, pages 115-116, Stamford, US; H. LIAO: "Table look-up realization of digital filtering";

ABSTRACT EP 378253 A2
A video transformation and filtering system generates for each source image data point a plurality of target image addresses indicating a displacement between a point at which the source image data point maps into the target image and each data point of the target image which is affected by the source image data point. By providing either sequentially or in parallel a separate processing for each target image data point that is affected by a current source image data point values for all of the target image data points can be generated from a single pass of the

source image data points. By effectively providing the filtering in the domain of the target image instead of the source image a single filter function with a fixed number of points in the target image domain can be used to attain low pass filtering of the resulting target image irrespective of the degree of size compression of the video image.
ABSTRACT WORD COUNT: 162

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	900718	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	900912	A3	Separate publication of the European or International search report
Change:	900912	A2	Obligatory supplementary classification (change)
Examination:	910227	A2	Date of filing of request for examination: 901222
Examination:	931103	A2	Date of despatch of first examination report: 930921
Change:	940112	A2	Representative (change)
*Assignee:	940112	A2	Applicant (transfer of rights) (change): AMPEX SYSTEMS CORPORATION (1591830) 401 Broadway M-S 3-35 Redwood City, California 94063-3199 (US) (applicant designated states: DE;FR;GB)
Change:	940112	A2	Designated Contracting States (change)
Change:	940608	A2	Inventor (change)
Grant:	940608	B1	Granted patent
Oppn None:	950531	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1134
CLAIMS B	(German)	EPBBF1	917
CLAIMS B	(French)	EPBBF1	1374
SPEC B	(English)	EPBBF1	15943
Total word count - document A			0
Total word count - document B			19368
Total word count - documents A + B			19368

...INTERNATIONAL PATENT CLASS: **G06F-015/68** ...

... **G06F-015/62**

...SPECIFICATION 340 has one input responsive to the master reset signal, *RST and the second input responsive to **the** **Q** output of latch 337. Latch 337 is clocked by signal SYSK while latches 335, 336 are clocked ...of luminance and chrominance data. The components 400, 402 form output FIFO 17 which couples to frame **store** 18. The input of FIFO component 400 is clocked in response to signal PIXLCK, pixel luminance clock...

28/5,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00373227
Processor array.
Feldrechner.
Processeur en reseau.
PATENT ASSIGNEE:
AMT(HOLDINGS) LIMITED, (1014030), 65 Suttons Park Avenue, Reading Berkshire RG6 1AZ, (GB), (applicant designated states:

AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Hunt, David John, 3 Moores Green Wokingham, Berkshire RG11 1QG, (GB)
Thorpe, Roger Thomas, 24 Avellino, Irvine CA 92714, (US)
Broughton, Andrew John, 23952 Dovekie Cr., Laguna Niguel CA 92677, (US)
LEGAL REPRESENTATIVE:
Rackham, Stephen Neil et al (35061), GILL JENNINGS & EVERY 53-64 Chancery Lane, London WC2A 1HN, (GB)
PATENT (CC, No, Kind, Date): EP 375401 A1 900627 (Basic)
APPLICATION (CC, No, Date): EP 89313368 891220;
PRIORITY (CC, No, Date): GB 8829622 881220
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-015/80**
CITED PATENTS (EP A): GB 1445714 A
CITED REFERENCES (EP A):
IEEE 1987 SOLID-STATE CIRCUITS CONFERENCE, vol. 30, 1st edition, February 1987, pages 198-199,399-400, IEEE, New York, US; R. GRONDALSKI: "A VLSI chip set for a massively parallel architecture"
INTERNATIONAL SYMPOSIUM ON NEW DIRECTIONS IN COMPUTING, 12th-14th August 1985, Trondheim, pages 278-283, IEEE, New York, US; KUMAR et al.: "An array architecture for high speed parallel processing";

ABSTRACT EP 375401 A1
A processor array comprises a number of interconnected processing elements (PE). Each processing element (PE) includes row and column select inputs connected via respective row and column select lines to a control unit (MCU) for the array. The row select inputs in each row and the column select inputs in each column are connected in common. The processing elements (PE) receive broadcast row and column data over the respective row and column select lines.
ABSTRACT WORD COUNT: 78

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	900627 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	910109 A1	Date of filing of request for examination: 901116
Withdrawal:	931222 A1	Date on which the European patent application was deemed to be withdrawn: 930701

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	248
SPEC A	(English)	EPABF1	2493
Total word count - document A			2741
Total word count - document B			0
Total word count - documents A + B			2741

INTERNATIONAL PATENT CLASS: **G06F-015/80**

...SPECIFICATION with branches extending to each processing element PE.
In use the control unit MCU distributes address and **row / column** data in the manner described below and also controls the functioning of the array by broadcasting control signals to the processing elements **PE** , to the decoder DEC and to the multiplexers MUX. Three bit addresses are output by the control unit MCU. The decoder DEC shown in detail in Figure 4, decodes these addresses to produce appropriate **row** or **column** select signals for the processing elements **PE** . The first stage of the decoder produces a unique 0 on the **row** or **column** select line of the **row** or **column** that is to be selected. The second stage provides the option of an alternative method of addressing the array in which all rows

or **columns** are selected. In any particular instruction the MCU either broadcasts data to the array, or receives data...

...line in Figure 1) the data paths between the MCU and the array are provided by single **bidirectional** buses which at different times carry data both to and from the array.
In addition to carrying...

28/5,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00364202
Motion recognition apparatus
Bewegungserkennungsgerat
Appareil de reconnaissance du mouvement
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;NL)
INVENTOR:
Omata, Satoshi, 1-5-101 Narusegaoka 1-chome, Machida-shi Tokyo, (JP)
Shimizu, Hiroshi, 8-608 Yonban-cho, Chiyoda-ku Tokyo, (JP)
Yamaguchi, Yoko, 6-6-203 Hakusan 2-chome, Bunkyo-ku Tokyo, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 339867 A2 891102 (Basic)
EP 339867 A3 910703
EP 339867 B1 960110
APPLICATION (CC, No, Date): EP 89303926 890420;
PRIORITY (CC, No, Date): JP 88102920 880426
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; NL
INTERNATIONAL PATENT CLASS: **G06F-015/18** ; G06K-009/62
CITED PATENTS (EP A): EP 220077 A; EP 288332 A; EP 183622 A
CITED REFERENCES (EP A):
BIOLOGICAL CYBERNETICS vol. 51, 1985, Heidelberg pages 325 - 333; OHSUGA et al.: "Entrainment of two coupled van der Pol oscillators by an external oscillation as a base of "Holonic Control"";

ABSTRACT EP 339867 A2
A motion-pattern recognition apparatus of this invention is an apparatus for recognizing the motion of an object contained in physical image data. The apparatus has an input circuit (1) arranged to photograph an object and input physical image data upon the object, an arithmetic circuit (104) connected to the input means for computing a vector indicative of a variation in the physical image data from the input physical image data, an image forming circuit (105) connected to the arithmetic circuit for forming an image corresponding to the motion of the object from the vector input from the arithmetic circuit in accordance with a predetermined rule, a memory circuit (106) for retrievably storing in advance different kinds of conceptualized meaning of motion, a retrieving circuit (102) connected to the image forming circuit and the memory circuit for retrieving a conceptualized meaning close to the image of the motion of the object on the basis of the image of the motion, and the rule altering circuit (103) connected to the retrieving circuit and the image forming circuit for altering the predetermined rule on the basis of the conceptualized meaning retrieved by the retrieving circuit. Since a loop is formed between the image forming circuit and the memory circuit, it is possible to form, in the image forming circuit, an image based on a more exact recognition of the

motion of the object. This loop is of a form analogous to the visual information processing inherent in living things.
ABSTRACT WORD COUNT: 253

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	891102 A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	910306 A2	Date of filing of request for examination: 901231
Search Report:	910703 A3	Separate publication of the European or International search report
Change:	910807 A2	Obligatory supplementary classification (change)
Examination:	930929 A2	Date of despatch of first examination report: 930813
Grant:	960110 B1	Granted patent
Lapse:	961016 B1	Date of lapse of the European patent in a Contracting State: AT 960110
Oppn None:	970102 B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1052
CLAIMS B	(English)	EPAB96	912
CLAIMS B	(German)	EPAB96	835
CLAIMS B	(French)	EPAB96	1008
SPEC A	(English)	EPABF1	11536
SPEC B	(English)	EPAB96	11563
Total word count - document A			12589
Total word count - document B			14318
Total word count - documents A + B			26907

INTERNATIONAL PATENT CLASS: **G06F-015/18** ...

...SPECIFICATION inter-hypercolumn interference. Let us suppose that the coefficients of seven interactions which input to a certain **PE** of VP 105 are plotted in the direction of a **vertical** axis with the direction of **column** as a **horizontal** axis. If every plotted point is on a smooth curve such as sine curve, the "image" hold...

...SPECIFICATION inter-hypercolumn interference. Let us suppose that the coefficients of seven interactions which input to a certain **PE** of VP 105 are plotted in the direction of a **vertical** axis with the direction of **column** as a **horizontal** axis. If every plotted point is on a smooth curve such as sine curve, the "image" hold...

28/5,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00345160
Circuit for sensing voltages beyond the supply voltage of the sensing circuit.
Schaltung zum Feststellen von Spannungen unterhalb der Versorgungsspannung von Sensorschaltungen.
Circuit pour detecter des tensions sous la tension d'alimentation de circuits de capteurs.
PATENT ASSIGNEE:
IXYS CORPORATION, (1115770), 2355 Zanker Road, San Jose California 95131-1109, (US), (applicant designated states: DE;FR;GB;IT;NL)

INVENTOR:
Arcus, Christopher G., 15272 Charmeran, San Jose California 95124, (US)
LEGAL REPRESENTATIVE:
Dipl.-Phys.Dr. Manitz Dipl.-Ing., Dipl.-W.-Ing. Finsterwald Dipl.-Ing. Gramkow Dipl.-Chem.Dr. Heyn Dipl.-Phys. Rotermund (100613), Morgan, B.Sc.(Phys.) Robert-Koch-Strasse 1, D-8000 Munchen 22, (DE)
PATENT (CC, No, Kind, Date): EP 346937 A1 891220 (Basic)
APPLICATION (CC, No, Date): EP 89111012 890616;
PRIORITY (CC, No, Date): US 208310 880617
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G01R-019/165; **G06F-015/46**
CITED PATENTS (EP A): DE 3537315 A; DE 3632178 A

ABSTRACT EP 346937 A1
A voltage sensing circuit wherein voltages that appear at first and second sensing nodes are converted into first and second currents which are proportional to their respective voltages. A comparing circuit compares the first current to the second current and generates a difference current proportional to the difference between the magnitudes of the two currents. A rectifier circuit rectifies the difference current, and the difference current is added to a reference current. The combined current is applied to the first input terminal of a comparator. The second input terminal of the comparator is coupled to a reference voltage, and the comparator indicates when the voltage created from the combined currents exceeds the reference voltage.
ABSTRACT WORD COUNT: 118

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	891220	A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	891227	A1	Date of filing of request for examination: 891026
Withdrawal:	930127	A1	Date on which the European patent application was deemed to be withdrawn: 920103

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	553
SPEC A	(English)	EPABF1	3987
Total word count - document A			4540
Total word count - document B			0
Total word count - documents A + B			4540

...INTERNATIONAL PATENT CLASS: **G06F-015/46**

...SPECIFICATION conditioning circuitry 45, filter circuits 47, and a clock driver 50.
Host communications circuitry 40 provides a **bidirectional serial** communication **link** on the DATA line with a protocol easily implemented by most microprocessors. During **normal** operation, with the RUN//PGM HIGH and CHIP ENABLE LOW, the host communication circuitry receives a 3-**bit serial** command word on the DATA line. Pulses on the WRITE line clock the data bits into the...

...handshake clock pulses appear on the READ line. In the programming mode, with RUN//PGM, LOW, 7- **bit serial** words are transmitted to chip 27 to set the subsystem's default conditions, sense input's set...

28/5,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

(c) 2002 European Patent Office. All rts. reserv.

00306062

Digital data processing system.

Digitales Datenverarbeitungssystem.

Systeme du traitement de donnees numeriques.

PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)

INVENTOR:
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514, (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)

LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)

PATENT (CC, No, Kind, Date): EP 300516 A2 890125 (Basic)
EP 300516 A3 890426
EP 300516 B1 931124

APPLICATION (CC, No, Date): EP 88200921 820521;

PRIORITY (CC, No, Date): US 266413 810522; US 266539 810522; US 266521 810522; US 266415 810522; US 266409 810522; US 266424 810522; US 266421 810522; US 266404 810522; US 266414 810522; US 266532 810522; US 266403 810522; US 266408 810522; US 266401 810522; US 266524 810522

DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE

RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)

INTERNATIONAL PATENT CLASS: **G06F-009/46 ; G06F-012/14**

CITED REFERENCES (EP A):
PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, Atlantic City, 1972, pages 417-429, Afips Press; G.S. GRAHAM et al.: "Protection-Principles and practice"
IDEM.
COMPCON SPRING'80, digest of papers, San Francisco, 25th-28th February 1980, pages 340-343, IEEE, New York, US; T.D. McCREERY: "The X-tree operating system: Bottom layer"
IDEM.
COMPUTER ARCHITECTURE NEWS, October 1980, pages 4-11; J. RATTNER et al.: "Object-based computer architecture"
A.S. TANENBAUM: "Structured computer organization", 1976, pages 264-268, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, US
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 3, August 1979, pages 1286-1289, New York, US; D.B. LOMET: "Regions for controlling the propagation of addressability in capability systems";

ABSTRACT EP 300516 A2

The system has memory storing data and instructions and processing means. Memory is organized into objects identified by unique identifiers (UIDs) comprising a logical allocation unit identifier (LAUID) and an object serial number (OSN) provided by an architectural clock, associated with an offset (O) and length (L) enabling logical addresses to be

derived. Instructions (SIN's) are in an intermediate level language - (SOP's = S - language operations). Associated names (NAME A, NAME B) point to name tables which identify subjects to which the processor may respond in relation to the instruction in question. Protection is afforded by restricting access to memory operations to a subject pertaining to the set of subjects pertaining to the object in question.

ABSTRACT WORD COUNT: 122

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	20000209	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931124, BE 19931124, FR 19940415, IT 19931124, LU 19940531, NL 19931124, SE 19931124,
Application:	890125	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890426	A3	Separate publication of the European or International search report
Examination:	891206	A2	Date of filing of request for examination: 891011
Examination:	920115	A2	Date of despatch of first examination report: 911202
Grant:	931124	B1	Granted patent
Lapse:	940713	B1	Date of lapse of the European patent in a Contracting State: SE 931124
Lapse:	940810	B1	Date of lapse of the European patent in a Contracting State: AT 931124, SE 931124
Change:	940810	B1	Representative (change)
Lapse:	940928	B1	Date of lapse of the European patent in a Contracting State: AT 931124, NL 931124, SE 931124
Oppn None:	941117	B1	No opposition filed
Lapse:	941130	B1	Date of lapse of the European patent in a Contracting State: AT 931124, BE 931124, NL 931124, SE 931124
Lapse:	950118	B1	Date of lapse of the European patent in a Contracting State: AT 931124, BE 931124, FR 940415, NL 931124, SE 931124
Lapse:	991020	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931124, BE 19931124, FR 19940415, IT 19931124, NL 19931124, SE 19931124,

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1018
CLAIMS B	(German)	EPBBF1	868
CLAIMS B	(French)	EPBBF1	1115
SPEC B	(English)	EPBBF1	154256
Total word count - document A			0
Total word count - document B			157257
Total word count - documents A + B			157257

INTERNATIONAL PATENT CLASS: **G06F-009/46** ...

... **G06F-012/14**

...SPECIFICATION and from IOS 116 to MEM 112 through MIO Bus 129. IOMC Bus 131 is comprised of **bi - directional** control signals coordinating operation of MEM 112 and IOS 116. IOS 116 also has an interface to...

10112 and IOS 10116. Other such independently operating processors, for example, special arithmetic processors such as an **array** processor, or multiple FU 10120's, may be added to the present CS 10110.
In this regard...onto MOD Bus 10144 or MIO Bus 10129 when, respectively, driver gate enable signal Drive Assembly to **Mod** Bus (DRVASYMOD) to ASYMOD 23040 or Drive Assembly to MIO Bus (DRVASYMIO) to ASYMIO 23042 are asserted...

28/5,K/16 (Item 16 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00306058
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bachman, Brett L., 214 W. Canton Street Suite 4, Boston Massachusetts 02116, (US)
Bernstein, David H., 41 Bay Colony Drive, Ashland Massachusetts 01721, (US)
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Jones, Thomas M. Jones, 300 Reade Road, Chapel Hill North Carolina 27514, (US)
Katz, Lawrence H., 10943 S. Forest Ridge Road, Oregon City Oregon 97045, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Pilat, John F., 1308 Ravenhurst Drive, Raleigh North Carolina 27609, (US)
Richmond, Michael S., Fearringtn Post Box 51, Pittsboro North Carolina 27312, (US)
Schleimer Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514, (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
Wallach, Walter, A., Jr., 1336 Medfield Road, Raleigh North Carolina 27607, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 290111 A2 881109 (Basic)
EP 290111 A3 890503
EP 290111 B1 931222
APPLICATION (CC, No, Date): EP 88200917 820521;
PRIORITY (CC, No, Date): US 266404 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS: **G06F-009/30**
CITED PATENTS (EP A): US 3902163 A
CITED REFERENCES (EP A):

COMPUTER ARCHITECTURE NEWS, October 1980, pages 4-11; J. RATTNER et al.: "Object-based computer architecture"
DIGEST OF PAPERS, COMPCON SPRING 1980, 20TH IEEE COMPUTER SOCIETY INTERNATIONAL CONFERENCE, San Francisco, California, 25th-28th February 1980, pages 340-343, IEEE, New York, US; T.D. McCREERY; "The X-tree operating system: bottom layer"
PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, 1972, pags 417-429, Afips Press, Atlantic City, N.J., US; G. SCOTT GRAHAM et al.: "Protection - Principles and practice";

ABSTRACT EP 290111 A2

A digital computer system has a memory system organized into objects (10213) for storing items of information and a processor for processing data in response to instructions. An object identifier code is associated with each object. The objects include procedure objects (10312, 10314, 10316) and data objects. The procedure objects contain procedures including the instructions (10344) and name tables (10350) associated with the procedures. The instructions contain operation codes and names representing data. Each name corresponds to a name table entry in the name table (10350) associated with the procedure. The name table for a name contains information from which the processor may determine the location and the format for the data (e.g. an operand) represented by the name.

ABSTRACT WORD COUNT: 123

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	20000209	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931222, BE 19931222, FR 19940513, IT 19931222, LU 19940531, NL 19931222, SE 19931222,
Application:	881109	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890503	A3	Separate publication of the European or International search report
Examination:	891220	A2	Date of filing of request for examination: 891026
Examination:	920115	A2	Date of despatch of first examination report: 911202
Grant:	931222	B1	Granted patent
Change:	940810	B1	Representative (change)
Lapse:	940928	B1	Date of lapse of the European patent in a Contracting State: NL 931222
Lapse:	941026	B1	Date of lapse of the European patent in a Contracting State: NL 931222, SE 931222
Lapse:	941117	B1	Date of lapse of the European patent in a Contracting State: AT 931222, NL 931222, SE 931222
Lapse:	941130	B1	Date of lapse of the European patent in a Contracting State: AT 931222, BE 931222, NL 931222, SE 931222
Oppn None:	941214	B1	No opposition filed
Lapse:	950118	B1	Date of lapse of the European patent in a Contracting State: AT 931222, BE 931222, FR 940513, NL 931222, SE 931222
Lapse:	991020	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931222, BE 19931222, FR 19940513, IT 19931222, NL 19931222, SE 19931222,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1044
CLAIMS B	(German)	EPBBF1	890
CLAIMS B	(French)	EPBBF1	1185
SPEC B	(English)	EPBBF1	154314
Total word count - document A			0
Total word count - document B			157433
Total word count - documents A + B			157433

INTERNATIONAL PATENT CLASS: **G06F-009/30**

...SPECIFICATION and operation of Process Structures 10210, VP State Block 10218 will be described next below.
C. Virtual **Processor** State Blocks and Virtual Process Creation (Fig. 102)
Referring again to Fig. 102, VP State Blocks 10218...be selected from input provided from JPD Bus 10142, MOD Bus 10144, and IOM Bus 10130. In **certain cases** , an FIU 20120 data input may comprise two thirty-two bit words, for example, when a cross...

28/5,K/17 (Item 17 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00306057
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581 , (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bachman, Brett L., 214 W. Canton Street Suite 4, Boston Massachusetts 02116, (US)
Bernstein, David H., 41 Bay Colony Drive, Ashland Massachusetts 01721, (US)
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Jones, Thomas M. Jones, 300 Reade Road, Chapel Hill North Carolina 27514, (US)
Katz, Lawrence H., 10943 S. Forest Ridge Road, Oregon City Oregon 97045, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Pilat, John F., 1308 Ravenhurst Drive, Raleigh North Carolina 27609, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514 , (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
Wells, Douglas, M., 106 Robin Road, Chapel Hill North Carolina 27514, (US)
LEGAL REPRESENTATIVE:
Pears, David Ashley et al (34761), REDDIE & GROSE 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 290110 A2 881109 (Basic)
EP 290110 A3 890412
APPLICATION (CC, No, Date): EP 88200916 820521;

PRIORITY (CC, No, Date): US 266401 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556
INTERNATIONAL PATENT CLASS: **G06F-012/06 ; G06F-009/30**
CITED PATENTS (EP A): FR 2408176 A; EP 10185 A; FR 2253422 A
CITED REFERENCES (EP A):
SYSTEMES-COMPUTERS-CONTROLS, vol. 10, no. 6, November/December 1979, pages 41-50, Scripta Publishing Co., Silver Spring, Maryland, US; K. TAMARU et al.: "A high-performance microcomputer PMCS"
COMPUTER ARCHITECTURE NEWS, October 1980, pages 4-11; J. RATTNER et al.: "Object-based computer architecture"
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 19, no. 1, June 1976, pages 67-70, New York, US; T.J. DVORAK et al.: "Hardware assist for microcode execution of storage-to-storage move instructions";

ABSTRACT EP 290110 A2
A digital computer system in which data storage is referred to by a descriptor comprising an object number (AON 27111) denoting a variable-length block of storage, an offset (OFF 27113) indicating how far into that block a desired data item begins, and a length field (LEN 27115) denoting the length of the desired data item. Separate means exist for manipulating each of the three descriptor portions, thus facilitating repetitive operations on related or contiguous operands. Various levels of microcode control are included. Each level of microcode control has its own stack (902-905) facilitating interrupts between levels. Stacks are duplicated in "secure stacks" (504) in memory to protect against loss of state data from the stacks.
ABSTRACT WORD COUNT: 119

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	881109	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890412	A3	Separate publication of the European or International search report
Examination:	891206	A2	Date of filing of request for examination: 891011
Examination:	920122	A2	Date of despatch of first examination report: 911205
Refusal:	931124	A2	Date on which the European patent application was refused: 930710

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1390
SPEC A	(English)	EPABF1	155314
Total word count - document A			156704
Total word count - document B			0
Total word count - documents A + B			156704

INTERNATIONAL PATENT CLASS: **G06F-012/06** ...
... **G06F-009/30**

...SPECIFICATION operates as a unitary structure. That is, a particular address provided to GRF 10354 will address corresponding **horizontal** segments of each of GRF 10354's three sections residing in AONP 20216, OFFP 20218, and LENP...

...connected from, respectively, MOD Bus 10144 and JPD Bus 10142. OFFMUX 20240 also has a fourth 5 **bit** data input connected from Bias Logic (BIAS) 20246 and LENP 20220, described further below, and fifth 16...

28/5,K/18 (Item 18 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00291721
Linear chain of parallel processors and method of using same.
Lineare Kette von Parallelprozessoren und Benutzungsverfahren davon.
Chaine lineaire de processeurs paralleles et sa methode d'utilisation de celle-ci.
PATENT ASSIGNEE:
Applied Intelligent Systems, Inc., (973900), 110 Parkland Plaza, Ann Arbor, Michigan 48103, (US), (applicant designated states: DE;FR;GB;NL)
INVENTOR:
Wilson, Stephen S., 366 Hilldale Ann Arbor, Michigan 48015, (US)
LEGAL REPRESENTATIVE:
Patentanwalte Viering & Jentschura (100641), Postfach 22 14 43, D-80504 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 293700 A2 881207 (Basic)
EP 293700 A3 891018
EP 293700 B1 950201
APPLICATION (CC, No, Date): EP 88108175 880520;
PRIORITY (CC, No, Date): US 57128 870601
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: **G06F-015/76**
CITED PATENTS (EP A): EP 6748 A; EP 150449 A
CITED REFERENCES (EP A):
IEEE CONFERENCE PROCEEDINGS OF THE 13TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE
COMPUTER
idem
idem
IEEE JOURNAL OF SOLID-STATE CIRCUITS
IEEE TRANSACTIONS ON COMPUTERS
IEEE TRANSACTIONS ON COMPUTERS;

ABSTRACT EP 293700 A2
A system (9) for processing data matrices such as images and spatially related data includes a plurality of neighborhood processing units (10a-10n; 30a-30h) connected in a linear chain with direct data communication links (11a-11n, 21a-21n) between adjacent processing units. A sequence of instructions are sent to the processing units by a single controller (27), whereby all neighborhood processing units in the system receive the same instruction at any given cycle in the instruction sequence. The width of the data matrix array is the same as a number of processors, so that there is one processor per column in the data matrix. The memory (13a-13n) associated with each processor (10a-10n) is external and large enough to hold the entire image or data matrix. The processors are able to operate arithmetically in a serial or parallel mode, where an efficient means is provided to transpose 8 x 8 bit submatrices between the two modes. An indirect addressing arrangement (43h, 55h, 130, 131) is provided which operates on byte-wide memories (13a-13h; 132) external to the processing units (130).
ABSTRACT WORD COUNT: 179

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 881207 A2 Published application (A1with Search Report ;A2without Search Report)
Change: 881214 A2 Representative (change)
*Assignee: 881214 A2 Applicant (transfer of rights) (change):

			Applied Intelligent Systems, Inc. (973900) 110 Parkland Plaza Ann Arbor, Michigan 48103 (US) (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
*Assignee:	881214	A2	Previous applicant in case of transfer of rights (change): EATON CORPORATION (218422) Eaton Center Cleveland Ohio 44114 (US) (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE), Applied Intelligent Systems, Inc. (973900) 110 Parkland Plaza Ann Arbor, Michigan 48103 (US) (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
Change:	890607	A2	Designated Contracting States (change)
Search Report:	891018	A3	Separate publication of the European or International search report
Examination:	900221	A2	Date of filing of request for examination: 891220
Examination:	910904	A2	Date of despatch of first examination report: 910717
Change:	940330	A2	Representative (change)
Grant:	950201	B1	Granted patent
Oppn None:	960124	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPBBF2	2110
CLAIMS B	(English)	EPBBF2	1660
CLAIMS B	(German)	EPBBF2	1436
CLAIMS B	(French)	EPBBF2	1840
SPEC A	(English)	EPBBF2	10950
SPEC B	(English)	EPBBF2	9901
Total word count - document A			13060
Total word count - document B			14837
Total word count - documents A + B			27897

INTERNATIONAL PATENT CLASS: **G06F-015/76**

...SPECIFICATION wide memories 13a-13n. Each individual processing unit is respectively associated with an individual single-bit-wide **column** by multiple **row** memory, e.g., processing unit 10i is associated with memory 13i. The processor units are shown in...

...example. Each neighborhood processing unit 10a-10n also connects to associated memories 13a-13n by means of **bidirectional** data transfer lines 12a-12n. Data input device 20 provides a stream of data to first processing...

...SPECIFICATION wide memories 13a-13n. Each individual processing unit is respectively associated with an individual single-bit-wide **column** by multiple **row** memory, e.g., processing unit 10i is associated with memory 13i. The processor units are shown in...

...example. Each neighborhood processing unit 10a-10n also connects to associated memories 13a-13n by means of **bidirectional** data transfer lines 12a-12n. Data input device 20 provides a stream of data to first processing...

28/5,K/19 (Item 19 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

(c) 2002 European Patent Office. All rts. reserv.

00246190

Random access memory circuits
Speicher mit wahlfreiem Zugriff
Memoire a acces selectif

PATENT ASSIGNEE:
ADVANCED MICRO DEVICES, INC., (328120), 901 Thompson Place P.O. Box 3453, Sunnyvale, CA 94088-3453, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Spak, Michael E., Route 1, Box 170, Kyle, Texas 78640, (US)
Tyl, Craig S., 11636 Parkfield Drive, Austin Texas 78758, (US)
Wottrich, Philip C., 7403 Scenic Brook Drive, Austin Texas 78736, (US)
LEGAL REPRESENTATIVE:
Sanders, Peter Colin Christopher et al (35571), BROOKES & MARTIN High Holborn House 52/54 High Holborn, London WC1V 6SE, (GB)

PATENT (CC, No, Kind, Date): EP 237337 A2 870916 (Basic)
EP 237337 A3 900606
EP 237337 B1 970108
APPLICATION (CC, No, Date): EP 87302084 870311;
PRIORITY (CC, No, Date): US 838993 860312
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-007/00** ; G11C-019/00
CITED PATENTS (EP A): US 3760368 A
CITED REFERENCES (EP A):
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 15, no. 9, February 1973, pages 2949-2950, Armonk, N.Y., US; KEMERER: "Bidirectional FET shift register"
IDEM
IDEM
FUNKSCHAU, vol. 49, no. 1, 1977, paes 47-54, Munich, DE; ANONYMOUS: "Das Schieberegister"
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 20, no. 12, May 1978, pages 5152-5155, Armonk, N.Y., US; HANNA: "Ordered table memory with random-access addressing"
IDEM;

ABSTRACT EP 237337 A2
Random access memory circuits.
A fracturable x-y random access memory array for performing pushing and popping of data and fracturing the array simultaneously at a common address includes a row fracture circuit responsive to row addresses to fracture the array in the Y-direction and a column fracture circuit responsive to column addresses for fracturing the array in the X-direction. A plurality of memory cells are stacked in a plurality of columns to form an x-y organization which can be randomly accessed in response to the row and column addresses. The memory cells are responsive to a shift control driver circuit for bidirectional shifting of data by either pushing data into or popping data from at any point within one of the plurality of randomly addressable column at the same row and column addresses used to fracture the array defining a fracture point. Data in all the memory cells in the array with addresses higher (or lower) than the fracture point shift and the memory cells with addresses lower (or higher) than the fracture point maintain their data unchanged. A unique memory cell is also provided which is formed of a pair of cross-coupled latches which includes means for controlling a bidirectional shift by switching off power to one of the cross-coupled latches.
ABSTRACT WORD COUNT: 214

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	001213 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19970108, BE 19970108, CH 19970414, LI 19970414, GR 19970108, IT 19970108, LU 19970331, SE 19970408,
Lapse:	20000126 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19970108, BE 19970108, GR 19970108, IT 19970108, SE 19970408,
Lapse:	001227 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19970108, BE 19970108, CH 19970108, LI 19970108, GR 19970108, IT 19970108, LU 19970331, SE 19970408,
Application:	870916 A2	Published application (A1with Search Report ;A2without Search Report)
Lapse:	20000209 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19970108, BE 19970108, GR 19970108, IT 19970108, LU 19970331, SE 19970408,
Change:	871007 A2	Inventor (change)
Search Report:	900606 A3	Separate publication of the European or International search report
Examination:	900822 A2	Date of filing of request for examination: 900625
Examination:	930317 A2	Date of despatch of first examination report: 930203
Grant:	970108 B1	Granted patent
Lapse:	971015 B1	Date of lapse of the European patent in a Contracting State: AT 970108
Lapse:	971203 B1	Date of lapse of the European patent in a Contracting State: AT 970108, BE 970108
Oppn None:	980107 B1	No opposition filed
Lapse:	980311 B1	Date of lapse of the European patent in a Contracting State: AT 970108, BE 970108, SE 970408
Lapse:	991020 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19970108, BE 19970108, IT 19970108, SE 19970408,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB97	1441
CLAIMS B	(German)	EPAB97	1267
CLAIMS B	(French)	EPAB97	1566
SPEC B	(English)	EPAB97	8280

Total word count - document A 0
Total word count - document B 12554
Total word count - documents A + B 12554
INTERNATIONAL PATENT CLASS: **G06F-007/00** ...

...SPECIFICATION it from a lower address. It should be understood to those skilled in the art that the **single** - **bit** memory cell B100 could be replaced by an eight-bit word of storage elements arranged in a **horizontal** **row** . In this case, the gates G42 and G43 would drive the eight bits in parallel. Similarly, the...

...As a result, words rather than bits would then be connected in a series chain in each **column** so as to permit **bidirectional** shifting between corresponding bit locations of adjacent words. It will also be noted that

the bottom of one **column** (**column** (0 slash)) and the top of the next **column** (**column** 1) are interconnected or linked by a shift line 27a and data lines 27b, 27c. This would be repeated for each of the **columns** in a given matrix.

The input/output circuit 28a for the column zero includes a sense amplifier...

28/5,K/20 (Item 20 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

(c) 2002 European Patent Office. All rts. reserv.

00227825

Test method and apparatus for cellular array processor chip.

Testverfahren und Gerat fur zellularen Feldprozessorchip.

Methode et appareil de test pour puce de processeur en reseau cellulaire.

PATENT ASSIGNEE:

ITT INDUSTRIES INC., (209950), 320 Park Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL)

INVENTOR:

Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)

LEGAL REPRESENTATIVE:

Klunker . Schmitt-Nilson . Hirsch (101001), Winzererstrasse 106, D-8000 Munchen 40, (DE)

PATENT (CC, No, Kind, Date): EP 228949 A2 870715 (Basic)
EP 228949 A3 890614

APPLICATION (CC, No, Date): EP 86402742 861210;

PRIORITY (CC, No, Date): US 808418 851212

DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **G06F-015/06 ; G06F-011/20 ; G06F-011/26**

CITED PATENTS (EP A): US 3813650 A; US 3813650 A; US 4541090 A; US 4541090 A; EP 102296 A; US 4191996 A

ABSTRACT EP 228949 A2

A cellular array processor chip includes a common bus communicating with the individual cells thereof. The common bus can be monitored during chip testing to detect the presence, or absence, of a defective cell. Each cell can be inactivated with respect to the common bus. During testing if the presence of a defective cell is determined to exist each cell is individually tested until a defective cell is located. That cell is inactivated and the chip testing is resumed until all defective cells are located and inactivated.

ABSTRACT WORD COUNT: 91

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870715	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	870826	A2	Representative (change)
Change:	871021	A2	Representative (change)
Change:	890322	A2	Representative (change)
Change:	890607	A2	Representative (change)
Change:	890607	A2	Obligatory supplementary classification (change)
Search Report:	890614	A3	Separate publication of the European or International search report
Withdrawal:	900801	A2	Date on which the European patent application was deemed to be withdrawn: 891215

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	358
SPEC A	(English)	EPABF1	25364

Total word count - document A 25722
Total word count - document B 0
Total word count - documents A + B 25722

INTERNATIONAL PATENT CLASS: **G06F-015/06** ...

... **G06F-011/20** ...

... **G06F-011/26**

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.
Figure 84 shows a cellular **processor array** with controller. The key elements of this **processor array** are the 4 by 4 matrix of array chips, numbers 13,000 to 13,006 which shows...
...The array chips in a column are connected by a vertical bus as 13,011 to a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...

...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/21 (Item 21 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00227824
Two-wire/three-port RAM for cellular array processor.
RAM-Speicher mit zwei Linien und drei Porten fur zellularen Feldprozessor.
Memoire RAM a deux lignes et trois portes pour processeur en reseau cellulaire.
PATENT ASSIGNEE:
ITT INDUSTRIES INC., (209950), 320 Park Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)
LEGAL REPRESENTATIVE:
Klunker . Schmitt-Nilson . Hirsch (101001), Winzererstrasse 106, D-8000 Munchen 40, (DE)
PATENT (CC, No, Kind, Date): EP 234147 A2 870902 (Basic)
EP 234147 A3 890607
APPLICATION (CC, No, Date): EP 86402741 861210;
PRIORITY (CC, No, Date): US 808393 851212
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-015/06** ; G11C-008/00
CITED PATENTS (EP A): US 3968480 A; US 4541076 A; EP 121763 A
CITED REFERENCES (EP A):
IEEE MICRO, December 1985, IEEE, pages 37-49; S.G. MORTON et al.: "ITT CAP - toward a personal supercomputer";

ABSTRACT EP 234147 A2
A multiport memory includes first and second signal lines. Each signal line can simultaneously and independently access a particular address during a read memory portion of a clock pulse whereas both signal lines are used to write data to one address during another portion of the clock pulse.
ABSTRACT WORD COUNT: 52

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870902 A2	Published application (A1with Search Report ;A2without Search Report)
Change:	871021 A2	Representative (change)
Change:	890322 A2	Representative (change)
Search Report:	890607 A3	Separate publication of the European or International search report
Change:	890607 A2	Obligatory supplementary classification (change)
Withdrawal:	900801 A2	Date on which the European patent application was deemed to be withdrawn: 891208

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	351
SPEC A	(English)	EPABF1	25391
Total word count - document A			25742
Total word count - document B			0
Total word count - documents A + B			25742

INTERNATIONAL PATENT CLASS: **G06F-015/06** ...

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.
Figure 84 shows a cellular **processor array** with controller. The key elements of this **processor array** are the 4 by 4 matrix of array chips, number 13,000 to 13,006 which shows...

...The array chips in a column are connected by a vertical bus as 13,011 to a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...

...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/22 (Item 22 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00227823
Cellular array processing apparatus with variable nesting depth vector processor control structure.
Zellularer Feldprozessor mit einer Vektorprozessorsteuerungsstruktur, die eine variable Verschachtelungstiefe aufweist.
Processeur en reseau cellulaire utilisant une structure de commande de processeur vectoriel a profondeur d'emboitement variable.
PATENT ASSIGNEE:
ITT INDUSTRIES INC., (209950), 320 Park Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)
LEGAL REPRESENTATIVE:
Klunker . Schmitt-Nilson . Hirsch (101001), Winzererstrasse 106, D-8000 Munchen 40, (DE)
PATENT (CC, No, Kind, Date): EP 231686 A2 870812 (Basic)
EP 231686 A3 890614

APPLICATION (CC, No, Date): EP 86402740 861210;
PRIORITY (CC, No, Date): US 808305 851212
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-015/06**
CITED PATENTS (EP A): EP 121763 A; EP 223690 A
CITED REFERENCES (EP A):
IEEE MICRO, December 1985, pages 37-49, IEEE; S.G. Morton et al.: "ITT CAP-toward a personal supercomputer"
ELECTRONICS, vol. 58, no. 49, 9th December 1985, pages 40-41, New York, US; ITT takes pared-down approach to wafer-scale ICs"
H.S. STONE et al.: "Introduction to computer architecture", 1975, pages 333-338, Science Research Associates, Inc.
IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-21, no. 5, October 1986, pages 820-826, IEEE, New York, US; S.G. MORTON et al.: "The dynamically reconfigurable CAP array chip I";

ABSTRACT EP 231686 A2
A processor cell is described that may be integrated with a multiplicity of dynamically reconfigurable 16-bit slices to enable and disable arbitrary collections of processing elements under software control according to the data that they are operating upon. The structure allows a collection of word sizes to be defined and then for certain processing elements to be enabled or disabled according to the data that they are operating upon. A slave mechanism is described wherein for words comprised of a multiplicity of slices the most significant slice is in control and the other slices are slaved or forced to go along with the operation of the most significant slice. This slaving is obtained automatically without the necessity to explicitly coordinate the operation of the multiplicity of slices cooperated together to form a word. The cell includes a Find and Lose operation wherein a scaler control means selects one from a multiplicity of processors satisfying some condition. The apparatus finds the first cell satisfying some condition and operates upon that processor cell when the operation upon that processor is completed, the apparatus looses that processor and then goes on to the next processor satisfying the condition and so on.
ABSTRACT WORD COUNT: 202

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870812	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	870819	A2	Representative (change)
Change:	871021	A2	Representative (change)
Change:	890322	A2	Representative (change)
Change:	890531	A2	Representative (change)
Search Report:	890614	A3	Separate publication of the European or International search report
Withdrawal:	900808	A2	Date on which the European patent application was deemed to be withdrawn: 891215

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	447
SPEC A	(English)	EPABF1	25339
Total word count - document A			25786
Total word count - document B			0
Total word count - documents A + B			25786

INTERNATIONAL PATENT CLASS: **G06F-015/06**

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.

Figure 84 shows a cellular **processor array** with controller. The key elements of this **processor array** are the 4 by 4 matrix of array chips, numbers 13,000 to 13,006 which shows...

...The array chips in a column are connected by a vertical bus as 13,011 to a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...
...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/23 (Item 23 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00227822
Cellular array processing apparatus employing multiple state logic for coupling to data buses.
Zellularer Feldprozessor mit Mehrzustandslogik zur Verbindung mit dem Datenbus.
Processeur en reseau cellulaire utilisant une logique a plusieurs etats pour le couplage vers des bus de donnees.
PATENT ASSIGNEE:
International Standard Electric Corporation, (202420), 320 Park Avenue, New York New York 10022, (US), (applicant designated states: FR;GB)
INVENTOR:
Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)
LEGAL REPRESENTATIVE:
Pothet, Jean et al , c/o ITT Data Systems France S.A. Tour Maine Montparnasse 33, avenue du Maine, F-75755 Paris Cedex 15, (FR)
PATENT (CC, No, Kind, Date): EP 236643 A2 870916 (Basic)
EP 236643 A3 890614
APPLICATION (CC, No, Date): EP 86402739 861210;
PRIORITY (CC, No, Date): US 808315 851212
DESIGNATED STATES: FR; GB
INTERNATIONAL PATENT CLASS: **G06F-015/06** ; H03K-019/173; **G06F-001/00**
CITED PATENTS (EP A): EP 84247 A; EP 84247 A; US 4438491 A; US 4438491 A
CITED REFERENCES (EP A):
INTERFACES IN COMPUTING, vol. 2, no. 3, August 1984, pages 249-258, Elsevier Sequoia, Amsterdam, NL; C. CAPADAY et al.: "Analogue-to-digital and digital-to-analogue 12-bit interfaces for direct digital control using an AIM-65 microcomputer";

ABSTRACT EP 236643 A2
Apparatus is described to enable the use of 5 level logic comprising an off state so that a collection of like devices may be connected on a common bus where any one of those devices may drive the bus as well as 4 logic levels being represented by 4 voltage levels on the bus. The voltage levels are received by a 2-bit A/D converter and are generated by a 2-bit D/A converter that has been optimized to minimize power dissipation. Furthermore, a means is disclosed wherein a collection of pins may be organized in a regular structure to minimize the on-chip interconnect wiring so that a multiplicity of external buses may be supported, being multiplexed into a single internal common bus. In addition, a means is disclosed wherein these pins may be dynamically configured to form a collection of 2-level and 4-level buses to suit the interfacing needs of the chip, wherein a trade off may be made between the number of voltage levels and the number of buses being connected to.

ABSTRACT WORD COUNT: 176

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870916 A2	Published application (A1with Search Report ;A2without Search Report)
Change:	890607 A2	Obligatory supplementary classification (change)
Search Report:	890614 A3	Separate publication of the European or International search report
Withdrawal:	900822 A2	Date on which the European patent application was deemed to be withdrawn: 891215

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	789
SPEC A	(English)	EPABF1	25381
Total word count - document A			26170
Total word count - document B			0
Total word count - documents A + B			26170

INTERNATIONAL PATENT CLASS: **G06F-015/06** ...
... **G06F-001/00**

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.
Figure 84 shows a cellular **processor array** with controller. The key elements of the **processor array** are the 4 by 4 matrix of array chips, numbers 13,000 to 13,006 which shows...

...The array chips in a column are connected by a vertical bus as 13,011 to a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...

...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/24 (Item 24 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00227821
Cellular array processing apparatus with on-chip RAM and address generator apparatus.
Zellularer Feldprozessor mit integriertem RAM-Speicher und Adressengenerator.
Processeur en reseau cellulaire comportant une memoire RAM integree et un generateur d'adresses.
PATENT ASSIGNEE:
ITT INDUSTRIES INC., (209950), 320 Park Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)
LEGAL REPRESENTATIVE:
Klunker . Schmitt-Nilson . Hirsch (101001), Winzererstrasse 106, D-8000 Munchen 40, (DE)
PATENT (CC, No, Kind, Date): EP 232641 A2 870819 (Basic)

EP 232641 A3 890614
APPLICATION (CC, No, Date): EP 86402738 861210;
PRIORITY (CC, No, Date): US 808314 851212
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-015/06**
CITED PATENTS (EP A): EP 226103 A
CITED REFERENCES (EP A):
IEEE MICRO, December 1985, pages 37-49, IEEE; S.G. MORTON; "ITT CAP - toward a personal supercomputer"
IEEE TRANSACTIONS ON COMPUTERS, vol. C-27, no. 2, February 1978, pages 144-156, IEEE; R.P. ROESSER; "Two-dimensional microprocessor pipelines for image processing";

ABSTRACT EP 232641 A2
In a cellular array processor at least two of the plurality of processors in a row cooperate together as an address generator so that large amounts of memory external to the array chip may be addressed and in addition so that an address may be generated onboard for use by the DRAM memory associated with each processor. Based on this structure, a memory with an internal organization that is 256-bits wide may be connected to 16 16-bit processors which would require 256 bits of data. In so doing, a vast number of pins are saved, that is 256 bits of data out of the memory and 256 bits of data into the processing cells by combining the processing cells and memory on the same chip. It is significant that exactly one design of a processing cell may provide both a data processing element and an address processing element. In this way, these cells are interchangeable to maximize the yield and reliability of the device. A single address from the address generator addresses the entire onboard DRAM so as to use the number of address generators required and to reduce the amount of address decode logic required as well as minimizing power dissipation in the DRAM portion of the chip.
ABSTRACT WORD COUNT: 213

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870819	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	871021	A2	Representative (change)
Change:	890322	A2	Representative (change)
Change:	890503	A2	Representative (change)
Search Report:	890614	A3	Separate publication of the European or International search report
Withdrawal:	900808	A2	Date on which the European patent application was deemed to be withdrawn: 891215

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	471
SPEC A	(English)	EPABF1	25379
Total word count - document A			25850
Total word count - document B			0
Total word count - documents A + B			25850

INTERNATIONAL PATENT CLASS: **G06F-015/06**

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.

Figure 84 shows a cellular **processor array** with controller. The key elements of this **processor array** are the 4 by 4 matrix of array chips, numbers 13,000 to 13,006 which shows...

...The array chips in a column are connected by a vertical bus as 13,011 to

a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...

...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/25 (Item 25 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2002 European Patent Office. All rts. reserv.

00227820
Cellular array processing apparatus employing dynamically reconfigurable vector bit slices.
Zellularer Feldprozessor mit dynamisch rekonfigurierbaren Vektorbitscheiben.
Processeur en reseau cellulaire utilisant des tranches de vecteurs reconfigurables dynamiquement.
PATENT ASSIGNEE:
ITT INDUSTRIES INC., (209950), 320 Park Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL;SE)
INVENTOR:
Morton, Steven Gregory, 39 Old Good Hill Road, Oxford, CT 06483, (US)
LEGAL REPRESENTATIVE:
Klunker . Schmitt-Nilson . Hirsch (101001), Winzererstrasse 106, D-8000 Munchen 40, (DE)
PATENT (CC, No, Kind, Date): EP 234146 A2 870902 (Basic)
EP 234146 A3 890705
APPLICATION (CC, No, Date): EP 86402737 861210;
PRIORITY (CC, No, Date): US 808392 851212
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: **G06F-015/06**
CITED PATENTS (EP A): US 4304002 A; US 4314349 A
CITED REFERENCES (EP A):
CONFERENCE PROCEEDINGS, THE 10TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, Stockholm, 1983, pages 379-386, IEEE, New York, US; G. GAILLAT: "The design of a parallel processor for image processing on-board satellites: an application oriented approach"
Idem
IEEE MICRO, December 1985, pages 37-49, IEEE, New York, US; S.G. MORTON et al.: "ITT CAP - toward a personal supercomputer"
ELECTRONICS, vol. 58, no. 49, 9th December 1985, pages 40-41, New York, US; "ITT takes pared-down approach to wafer-scale ICs"
1986 PROCEEDINGS FALL JOINT COMPUTER CONFERENCE, Dallas, Texas, 2nd-6th November 1986, pages 277-286, IEEE, New York, US; S.G. MORTON: "A fault tolerant, BIT-parallel, cellular array processor";

ABSTRACT EP 234146 A2
There is described a cellular array including a matrixed array of processing elements. The processing elements are controlled by software to overcome manufacturing defects to cooperate together to form words of varying size and to replace cells that become defective during the lifetime of the processor, thereby prolonging its life. These cells communicate with memory external to the chip via a time divisioned multiplex bus. The bus is 32-bits wide and each cell is connected to both the upper half and lower half of the bus. According to the configuration bits that are loaded into a cell, the cell will communicate over the top half or the bottom half of the bus according to the significance of the

bits placed in the cells and may form words between 16-bits and 246-bits in the case where 20 such cells are implemented on a single chip with four of the cells being deemed to be spare parts. For simplicity, typical word sizes would be 2n x 16 bits although in principle any multiple of 16-bits may be obtained. Each cell contains a 16-bit multiport RAM which provides general purpose registers for use by the programmer as well as systems registers such as the processor status word and multiplier quotient register as well as a full-function arithmetic logic unit, as well as path logic to connect the cells together and control means to control the flow of information through the path logic according to the instruction being executed. This chip may be considered to implement a vector bit slice part in that a collection of 16-bit slice elements is contained on a single chip. These cells operate in a single instruction multiple data format as 16 16-bit processors, 8 32-bit processors, and so on, operating on the same instruction stream simultaneously but with different data streams.

ABSTRACT WORD COUNT: 307

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	870902	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	871021	A2	Representative (change)
Change:	890322	A2	Representative (change)
Change:	890503	A2	Representative (change)
Change:	890531	A2	Representative (change)
Search Report:	890705	A3	Separate publication of the European or International search report
Withdrawal:	900905	A2	Date on which the European patent application was deemed to be withdrawn: 900106

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	660
SPEC A	(English)	EPABF1	25391
Total word count - document A			26051
Total word count - document B			0
Total word count - documents A + B			26051

INTERNATIONAL PATENT CLASS: **G06F-015/06**

...SPECIFICATION operation of the Vector IF/ELSE instruction is explained in Figure 86.

Figure 84 shows a cellular **processor array** with controller. The key elements of this **processor array** are the 4 by 4 matrix of array chips, numbers 13,000 to 13,006 which shows...

...The array chips in a column are connected by a vertical bus as 13,011 to a **vertical memory** as 13,007. The cells in these array chips share this **vertical memory** on a time division multiplex basis, first between the chips and then between the cells within a...

...would typically be connected to the horizontal memory and the Y bus is typically connected to the **vertical memory** . Connections between adjacent chips are made by the left/right connections as 13,013 and the right...

28/5,K/26 (Item 26 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

(c) 2002 WIPO/Univentio. All rts. reserv.

00917520

A METHOD FOR DELIVERING DATA OR CODE SEGMENTS TO A LOCAL COMPUTER INA

DISTRIBUTED COMPUTER NETWORK

PROCEDE PERMETTANT D'ACHEMINER DES DONNES OU DES SEGMENTS DE CODE VERS UN ORDINATEUR LOCAL DANS UN RESEAU INFORMATIQUE PARTAGE

Patent Applicant/Inventor:
PALUMBO Fabio, Via Satolli, 45, I-00100 Roma, IT, IT (Residence), IT (Nationality)
IANNICCA Marcovalerio, Via Sistina, 134, I-00100 Roma, IT, IT (Residence), IT (Nationality)
Legal Representative:
MARIETTI Giuseppe (agent), Marietti E Gislon S.r.l., Via Larga, 16, I-20122 Milano, IT,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200250711 A1 20020627 (WO 0250711)
Application: WO 2000IT516 20001213 (PCT/WO IT0000516)
Priority Application: WO 2000IT516 20001213
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-017/30**
Publication Language: English
Filing Language: Italian
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 5777

English Abstract
The invention relates to a method for supplying data and/or code segments to a local computer, in a distributed computer network, during loading of a first page of information present on a remote computer belonging to said network and requested by said local computer, said first page including a plurality of sequential commands for a read/execute program resident on said local computer, comprising the steps of: reading, by said read/execute program, of a linking command present on said first page being loaded, said command not coinciding with the last information contained in the first page; execution of said linking command by the read/execute program, said command causing momentary interruption of loading of the first page and start of loading of an executable object external to the first page; execution of said external object containing the data and/or the code segments to be supplied: during the step of execution of said object, simultaneous loading of the subsequent command/commands or information of said first page.

French Abstract
L'invention porte sur un procede permettant de fournir des donnees et/ou des segments de code a un ordinateur local dans un reseau informatique partage pendant le chargement d'une premiere page d'information se trouvant sur un ordinateur a distance faisant partie dudit reseau et demandee par ledit ordinateur local. Cette premiere page contient une pluralite de commandes sequentielles pour un programme de lecture/execution residant sur ledit ordinateur local. Le procede de cette invention comprend les etapes suivantes: la lecture effectuee par le programme de lecture/execution d'une commande de liaison presente sur ladite premiere page en cours de chargement, ladite commande ne coincidant pas avec la derniere information contenue dans la premiere page. L'execution de ladite commande de liaison assuree par le programme

de lecture/execution, ladite commande provoquant une interruption momentanee du chargement de la premiere page et le debut du chargement d'un objet executable non compris dans la premiere page; l'execution dudit objet externe contenant les donnees et/ou les segments de code a fournir; et le chargement simultane pendant l'execution dudit objet, de la commande/commandes posterieure(s) ou l'information de ladite premiere page.

Legal Status (Type, Date, Text)
Publication 20020627 A1 With international search report.

Main International Patent Class: **G06F-017/30**
Fulltext Availability:
Claims

Claim
... and to the loading/execution of the new page in window 9. Table I further comprises a **column** regarding the display on the screen of the local computer 202. As far as the loading of...

...for loading the requested page.
EXAMPLE
In a local computer connected to Internet by means of a **normal** telephone line with a 38,000-KbPS modem there is loaded a first page in HTML format...

28/5,K/27 (Item 27 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00885021 **Image available**
METHOD AND APPARATUS FOR CONNECTING A MASSIVELY PARALLEL PROCESSOR ARRAY TO A MEMORY ARRAY IN A BIT SERIAL MANNER
PROCEDE ET APPAREIL DE CONNEXION DU RESEAU D'UN ORDINATEUR MASSIVEMENT PARALLELE A UN RESEAU DE MEMOIRE EN SERIE PAR BIT
Patent Applicant/Assignee:
MICRON TECHNOLOGY INC, 8000 S. Federal Way, Boise, ID 83707-0006, US, US (Residence), US (Nationality)
Inventor(s):
KIRSCH Graham, 2 Ringshall Gardens, Bramley, Tadley, Hants RG26 5BW, GB,
Legal Representative:
GREGORY Donald A (agent), Dickstein, Shapiro Morin & Oshinsky LLP, 2101 L Street NW, Washington, DC 20037-1526, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200219129 A2 20020307 (WO 0219129)
Application: WO 2001US27047 20010831 (PCT/WO US0127047)
Priority Application: US 2000652003 20000831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-015/16**
Publication Language: English
Filing Language: English
Fulltext Availability:

Detailed Description
Claims
Fulltext Word Count: 10308

English Abstract
A method and apparatus for connecting the processor array of an MPP array to a memory such that data conversion by software is not necessary, and the data can be directly stored in either a normal mode or vertical mode in the memory is disclosed. A connection circuit is provided in which multiple PEs share their connections to multiple data bits in the memory array. Each PE is associated with a plurality of memory buffer registers, which stores data read from (or to be written to) one or two memory data bits. In horizontal (normal) mode connection the memory bits are selected so that all the bits of a given byte are stored in the same PE, i.e., each set of buffer registers associated with a respective PE contains one byte as seen by an external device. In vertical (bit serial) mode, each set of buffer registers contains the successive bits at successive locations in the memory corresponding to that PEs position in the memory word. The selection is achieved utilizing a multiplexer on the input to the register and a pair of tri-state drivers which drive each data line.

French Abstract
L'invention concerne un procede et un appareil de connexion du reseau d'un ordinateur massivement parallele (MPP) a une memoire sans necessite de convertir les donnees a l'aide d'un logiciel, celles-ci pouvant etre directement stockees dans la memoire soit en mode normal, soit en mode vertical. Un circuit de connexion comprend de multiples elements de traitement partageant leurs connexions a de multiples bits de donnees du reseau de memoire. Chaque element de traitement est associe a plusieurs registres tampons de memoire de stockage des donnees lues dans (ou destinees a etre ecrites dans) un ou deux bits de donnees de memoire. Dans une connexion en mode horizontal (normal), les bits de memoire sont selectionnes de maniere que tous les bits d'un octet donne soient stockes dans le meme element de traitement, c'est-a-dire que chaque ensemble de registres tampons associes a un element de traitement correspondant contient un octet tel que visualise par un dispositif externe. En mode vertical (en serie), chaque ensemble de registres tampons contient les bits successifs a des emplacements successifs de la memoire correspondant a la position de l'element de traitement dans le mot memoire. La selection s'effectue a l'aide d'un multiplexeur sur l'entree du registre et une paire de pilotes a trois etats commandant chaque ligne de donnees.

Legal Status (Type, Date, Text)
Publication 20020307 A2 Without international search report and to be republished upon receipt of that report.
Examination 20020510 Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **G06F-015/16**
Fulltext Availability:
Detailed Description

Detailed Description
... are simple, it is possible to clock them fastiand without resorting to deep pipelines.

In one exemplary **massively** parallel **processor array** , each **PE** 16 in the
PE array 14 uses only a single pin to connect to the memory 12. Thus, a one bit...

...value are stored at successive locations in the memory 12. This storage format is referred to as " **vertical** " **storage** . Thus data read from and written to each **PE** will be read ...successive locations in the memory 12 as illustrated in Fig. 4. Thus, in Fig. 4, if each **PE** 16a - 16n in a row 22 of **PE** array 14 is an eight bit **PE** ., i.e., it operates on eight bits of data at a time,) the data in the memory will be stored in eight successive vertical locations as illustrated. As noted above) each **PE** is connected to memory 12 by a one bit wide data connection 24. Thus, data from **PE** 16c will be stored in a byte sized area 20 of memory 12 in successive locations in...

...storage of data bit serially has a number of benefits. First, die number of data wires per **PE** 16 to the memory 12 is kept to a minimum. Second, it allows for variable precision arithmetic...

...and processed efficiently. Third, in some cases, the difference in speed of the memory access versus the **PE** cycle time can be matched by serializing the data access. There are some drawbacks, however, with storing...read from a memory to a PE and written to the memory from the PE via a **single bit** connection in either a **vertical** or **horizontal mode** .

The use of a single register 52, such as for example 52a-52h, for each circuit 40a...

28/5,K/28 (Item 28 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00805565 **Image available**
DISPLAY SYSTEM
SYSTEME D'AFFICHAGE
Patent Applicant/Assignee:
TELEFONAKTIEBOLAGET LM ERICSSON (publ), S-126 25 Stockholm, SE, SE (Residence), SE (Nationality)
Inventor(s):
LUTNAES Sturla, Ullerakersvagen 64, S-746 43 Uppsala, SE,
Legal Representative:
HEDBERG Ake (et al) (agent), Aros Patent AB, P.O. Box 1544, S-751 45 Uppsala, SE,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200139167 A1 20010531 (WO 0139167)
Application: WO 2000SE2179 20001108 (PCT/WO SE0002179)
Priority Application: SE 994271 19991125
Designated States: AE AG AL AM AT AT (utility model) AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ CZ (utility model) DE DE (utility model) DK DK (utility model) DM DZ EE EE (utility model) ES FI FI (utility model) GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KR (utility model) KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SK (utility model) SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G09G-003/36
International Patent Class: **G06F-001/32**
Publication Language: English
Filing Language: English
Fulltext Availability:

Detailed Description
Claims
Fulltext Word Count: 4640

English Abstract
According to the present invention, in an electronics device having a display unit (11), the display unit (11) comprises according to the present invention at least two interfaces (38, 39), controlled by one display control unit (30, 31) each. The electronics device comprises further an arbitrator (42), resolving any access conflicts between the interfaces (30, 31). The arbitrator (42) can be implemented as a switching means in the display unit or as a software communication between the display control units. The interfaces (30; 31) preferably control mutually overlapping areas (40, 41) of the display unit (11). One of the interfaces (39) may be slow, and accessed e.g. by a serial connection, being responsible for the information display during stand-by or inactivity periods, when only limited information display is needed. During such periods, the display control device (31) for the other interface (38) and associated circuitry are preferably turned off. The other interface (38) is preferably of a fast type, accessed by e.g. a parallel connection, being responsible for a full utilization of the display unit (11).

French Abstract
Selon l'invention, dans un dispositif electronique comprenant une unite d'affichage (11), cette unite d'affichage (11) comprend au moins deux interfaces (38, 39), commandees chacune par une unite de commande d'affichage (30, 31). Ce dispositif electronique comprend egalement un arbitre (42) destine a resoudre les conflits d'acces entre les interfaces (30, 31). Cet arbitre (42) peut etre mis en oeuvre en tant que dispositif de commutation dans l'unite d'affichage ou en tant que communication de logiciel entre les unites de commande d'affichage. De preference, ces interfaces (30; 31) commandent des zones (40, 41) de l'unite d'affichage (11) qui se chevauchent. Une des interfaces (39), qui peut etre lente et connectee par exemple, au moyen d'un branchement en serie, est responsable de l'affichage d'informations pendant des periodes d'attente ou d'inactivite, lorsque seules des informations limitees sont requises. Pendant ces periodes, le dispositif de commande d'affichage (31) pour l'autre interface (38) et ses circuits associes sont, de preference, eteints. L'autre interface (38), qui est de preference d'un type rapide et connectee, par exemple, au moyen d'un branchement en parallele, est responsable d'une utilisation complete de l'unite d'affichage (11).

Legal Status (Type, Date, Text)
Publication 20010531 A1 With international search report.

International Patent Class: **G06F-001/32**
Fulltext Availability:
Detailed Description

Detailed Description
... unit according to the present invention. A LCD unit 1 1 comprises a LCD area 53.

A **row** driver 82 and a **column** driver 81 control the LCD area 53. The **column** driver is comprised in a driver control unit 80. A first interface 39 and a second interface...
...this embodiment constituted as a serial interface, having a serial data input/output connection 83 and a **serial** clock **connection** 84. The second interface 38 is in this embodiment constituted as

a parallel interface, having a 16 bit **bi - directional** data bus 85, a command/data select signal connection 86, a read strobe connection 87 and a...

28/5,K/29 (Item 29 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00784185 **Image available**
A SYSTEM AND METHOD FOR STREAM-BASED COMMUNICATION IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE DE PRODUCTION FOURNISSANT UN SYSTEME DE COMMUNICATION EN CONTINU DANS UN ENVIRONNEMENT DE CONFIGURATIONS DE SERVICES DE COMMUNICATION
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200117195 A2-A3 20010308 (WO 0117195)
Application: WO 2000US24125 20000831 (PCT/WO US0024125)
Priority Application: US 99386717 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-029/06
International Patent Class: **G06F-017/22** ; H04L-029/12
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150532

English Abstract
A system, method, and article of manufacture are disclosed for providing a stream-based communication system. A shared format is defined on interface code for a sending system and a receiving system. A message to be sent from the sending system to the receiving system is translated based on the shared format. Once translated, the message is then sent from the sending system and received by the receiving system. Once the message is received by the receiving system, the message is then translated based on the shared format.

French Abstract
L'invention concerne un systeme, un procede et un article de production fournissant un systeme de communication en continu. Un format partage est defini selon un code d'interface pour un systeme emetteur et un systeme recepteur. Un message devant etre envoye par le systeme emetteur est traduit sur la base du format partage. Une fois traduit, le message est

envoye du systeme emetteur et recu par le systeme recepteur. Le message recu par le systeme recepteur est ensuite traduit sur la base du format partage.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010907 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011115 Late publication of international search report
Republication 20011115 A3 With international search report.

International Patent Class: **G06F-017/22** ...
Fulltext Availability:
Detailed Description

Detailed Description
... to utilize each others capabilities or functions. This is generally done by assuming a common component object **model** on which to build the architecture. It is worthwhile to differentiate between an object and a class...applications
Digital Equipment Corp.'s DEC/EDI
Sterling Commerce's GENTRAN
EDI value-added networks (VANs) - VANs **link** EDI trading partners and transmit EDI
messages through a central electronic clearinghouse
IBM Global Services' Advantis
GE...

28/5,K/30 (Item 30 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00784131
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A MULTI-OBJECT FETCH COMPONENT IN AN INFORMATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE MANUFACTURE POUR COMPOSANT DE RECUPERATION MULTI-OBJET DANS UN ENVIRONNEMENT CARACTERISE PAR DES SERVICES D'INFORMATIONS
Patent Applicant/Assignee:
ANDERSEN CONSULTING LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918 , US,
Legal Representative:
HICKMAN Paul L (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116723 A2 20010308 (WO 0116723)
Application: WO 2000US24083 20000831 (PCT/WO US0024083)
Priority Application: US 99386238 19990831
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: **G06F-009/44**
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 150940

English Abstract
A system, method, and article of manufacture are provided for retrieving muliple business objects across a network in one access operation. A business object and a plurality of remaining objects are provided on a persistent store. Upon receiving a request for the business object, it is established which of the remaining objects are related to the business object. The related objects and the business object are retrieved from the persistant store in one operation and it is determined how the retrieved related objects relate to the business object and each other. A graph of relationships of the business and related objects is instantiated in memory.

French Abstract
La presente invention concerne un systeme, un procede et un article manufacture destine a la recuperation de plusieurs objets d'affaires dans un reseau en une operation d'acces. A cet effet, on dispose dans une memoire permanente d'un objet d'affaire et d'une pluralite d'objets restants. Des la reception d'une requete se rapportant a un objet d'affaires, on recherche deux des objets restants qui sont en relations avec l'objet d'affaires. Une seule operation permet ainsi de recuperer dans la memoire permanente ces objets ainsi que l'objet d'affaires. Il ne reste plus qu'a determiner les relations existant d'une part entre les objets consideres et d'autre part entre ces objets et l'objet d'affaires. Une instanciation d'un graphique des relations entre les objets et l'objet d'affaire est conservee en memoire.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010809 Request for preliminary examination prior to end of 19th month from priority date

Main International Patent Class: **G06F-009/44**
Fulltext Availability:
  Detailed Description

Detailed Description
... interface devices such as a touch screen (not shown) to the bus 112, communication adapter 134 for **connecting** the workstation to a communication network (e.g., a data processing network) and a display adapter 136...the Unix client/server RDBMS market, Oracle is available for a wide variety of hardware platforms including **MPP** machines. Oracles market position and breadth of platforin support has made it the RDBMS of choice for...of developers to do things consistently and to benefit from previously captured, reusable knowledge.

capital.

Business Components **model** the business. It sounds straightforward, but even with experience it's a challenge to identify the right...

28/5,K/31 (Item 31 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00565053 **Image available**

WALLET FOR PERSONAL INFORMATION DEVICE
PORTEFEUILLE POUR DISPOSITIF ELECTRONIQUE PERSONNEL

Patent Applicant/Assignee:
XIRCOM INC,
KAVANAUGH Paul K,
TODOROVICH Mark M,
GRIEB Robert L,
Inventor(s):
KAVANAUGH Paul K,
TODOROVICH Mark M,
GRIEB Robert L,

Patent and Priority Information (Country, Number, Date):
Patent: WO 200028426 A1 20000518 (WO 0028426)
Application: WO 99US26626 19991111 (PCT/WO US9926626)
Priority Application: US 98189572 19981111
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-013/10**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 11121

English Abstract

A wallet (70) for a personal information device (10) in a form of a PCMCIA card such as a PCMCIA-card electronic organizer. The wallet (70) includes an input device (80) separated from the input device (14) of the personal information device (10) and two halves (72, 74) that may be folded together in a wallet-like fashion. One (72) of the halves generally includes a touch panel input (80) to allow a user to enter information, commands instructions, etc., thereto. A personal information device (10) is mounted to the second half (74) of the wallet (70). When mounted, the wallet (70) supplies via an electrical connection (16) or induction communication (84) the user-supplied information entered into the touch panel input (80) to the personal information device (10). The wallet display (80) may be powered by personal information device (10) via the electrical connection or self-powered. Upon coupling the personnal information device (10) to the wallet (70), personal information device (10) may supply a wake signal to wake up or automatically turn on the input device (80) of the wallet (70). The wallet (70) may further include an input/output connector (82) for coupling via a cable (90) the wallet (70) to an external device such as another wallet, a personal computer, etc.

French Abstract

L'invention se rapporte a un portefeuille (70) concu pour un dispositif electronique personnel (10) se presentant sous la forme d'une carte PCMCIA, tel qu'un agenda electronique a carte PCMCIA. Ce portefeuille (70) comporte un organe d'entree (80) distinct de l'organe d'entree (14) du dispositif electronique personnel (10) et presente deux moities (72, 74) qui peuvent se refermer l'une sur l'autre a la maniere d'un portefeuille. L'une (72) de ces moities comporte generalement un organe

d'entree de type panneau a effleurement (80) qui permettent a un utilisateur d'y entrer des informations, des commandes, des instructions, etc. Lorsqu'il est assemble, ce portefeuille (70) transmet au dispositif electronique personnel (10) les informations fournies par l'utilisateur et entrees au moyen du panneau a effleurement (80), par l'intermediaire d'une connexion electrique (16) ou d'un organe de communication par induction (84). L'ecran (80) du portefeuille peut etre alimente par le dispositif electronique personnel (10) par l'intermediaire d'une connexion electrique ou etre auto-alimente. Lorsqu'il est couple au portefeuille (70), le dispositif electronique personnel (10) peut delivrer un signal de reveil permettant d'activer ou de mettre automatiquement sous tension l'organe d'entree (80) du portefeuille (70). Ce dernier peut egalement comporter un connecteur d'entree/sortie (82) destine au couplage, par l'intermediaire d'un cable (90), du portefeuille (70) a un dispositif externe tel qu'un autre portefeuille, un ordinateur personnel, etc.

Main International Patent Class: **G06F-013/10**
Fulltext Availability:
Claims

Claim
... to an integrated circuit mounted on the reverse side of the touchpad, the first (upper) layer containing **vertical** electrode strips and the second (lower) layer containing **horizontal** electrical strips. Mutual capacitance from each of the **horizontal** electrodes to each of the **vertical** electrodes, and which is modified by the presence of a human finger, is measured by the touchpad...
...embodiments previously discussed. Referring back to Fig. 9, and as previously mentioned, wallet 70 may include a **serial connector** 82 to which a cable 90 may be coupled for the purpose of interfacing personal information device...

...0, when inserted into wallet 70, to a host computer. Cable 90 may include attached thereto a **serial connector** or other type of connector, (not shown) that may be **connected** to the **serial** or other port of the host computer. Cable 90 may even be attached to a PCMCIA card ...

...that is not reflected in the host computer. In accordance with another embodiment of the present invention, **serial connector** 82 of wallet 70 may be coupled via cable 90 (or other suitable cable) to any one...a different shape and size (e.g., a three-fold type wallet, a wallet with folds along **perpendicular** axes, etc.). Therefore, it is intended that the appended claims be interpreted as including the embodiments described ...

28/5,K/32 (Item 32 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00552002 **Image available**
DESIGN TOOL
OUTIL DE CONCEPTION
Patent Applicant/Assignee:
ASKO INC,
Inventor(s):
ZELT Albert R III,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200015375 A1 20000323 (WO 0015375)

Application: WO 99US20763 19990910 (PCT/WO US9920763)
Priority Application: US 98150523 19980910
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: B23D-035/00
International Patent Class: **G06F-017/50**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 11300

English Abstract

A design tool for predictively indicating, in metal slitting, expected edge conditions of slit metal. Also contemplated is a corresponding method. Further contemplated is a design tool and method for providing, in metal slitting, a predictive assessment of at least one condition relating to at least one of: knife edge and slit metal edge.

French Abstract

L'invention concerne un outil de conception destine a indiquer a l'avance, au cours d'operations de refendage de metaux, des etats attendus relatifs aux bords du metal refendu. L'invention concerne egalement le procede correspondant. L'invention concerne enfin un outil et un procede de conception permettant, au cours des operations de refendage des metaux, d'evaluer a l'avance au moins un etat relatif soit a l'arete du couteau soit au bord du metal refendu.

International Patent Class: **G06F-017/50**
Fulltext Availability:
Claims

Claim
... 5
Slitter Knive
Top Arbor
Shoulder Arbor Lockir
C3
Female e
CA
C
to
U) acer
I **Vertical**
M VTAf 2 1 ------- @j ---- - --------------
M Clearance
:C:
M or Overlap Hofizont
M
Clearan
pace
r
M
Female

Bo Arbor A ckj
Shoulder

FIGO
(Prior Art)
c **Horizontal** tep
Clearance
Lower Knife
Knih
FIG= 2A
(Prior Art)
Step @
At instant of "parring"
Knife
Ni
Knife...

...Knife
Break
&t@@Break
Knife
FIGm 2C
(Prior Art)
SUBSTITUTE SHEET (RULE 26)
Slitter Knives
Edge View
(**Vertical**
Clearance)
C C
C
(**Horizontal**
Clearance)
H
Li
Case 2 Case 3
Case 1 **Vertical** **Vertical**
Vertical Clearance or Overlap
Clearance Overlap
FIGm 3
(Prior Art)
SUBSTITUTE SHEET (RULE 26)
Slitter Knives
Top Arbor
Shoulder
Arbor Nut
Fema Male Female
Stripper Stripper Stripper
Ring Ring Ring
C
C
Male **Horizontal**
Stripper Clearance
Ring
Bottom or Spacer
Shoulder
FIG 4
(Prior Art)
SUBSTITUTE SHEET (RULE 26)
Des@qn...

...4
f YFF F
OK I Refresbi
FIGm 6 40

2002 2004
Dull Gray Fracture Zone Dull
Straight Line Between Shiny Jagg,
Penetration Zone and Fracture Penetr;
C
M
Cn Shiny Penetration Zone is Ev
M...

...0.000 2 0.5 0.003 3857.813 IS-1
M
Wic
F6A
Wei
M
rij
Pe
E
Setup: Head I-Standard Setup) 8/13/9B
FIGO 10
E 1.25 'CO
E
1...

28/5,K/33 (Item 33 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00522061 **Image available**
PATTERN GENERATION AND SHIFT PLANE OPERATIONS FOR A MESH CONNECTED COMPUTER
GENERATION DE MOTIF ET OPERATIONS DE DEPLACEMENT DE PLAN POUR ORDINATEUR A ARCHITECTURE EN RESEAU
Patent Applicant/Assignee:
LOCKHEED MARTIN CORPORATION,
Inventor(s):
MEEKER Woodrow L,
ABERCROMBIE Andrew P,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9953413 A1 19991021
Application: WO 99US7004 19990409 (PCT/WO US9907004)
Priority Application: US 9857469 19980409
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-015/80**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13116

English Abstract
An apparatus for processing data has a Single-Instruction-Multiple-Data (SIMD) architecture, and a number of features that improve performance and programmability. The apparatus includes a rectangular array of processing elements and a controller. The apparatus offers a number of techniques for shifting image data within the array. A first technique,

the ROLL option, simultaneously shifts image planes in **opposite directions** within the array. A second technique, the gated shift option, makes a **normal** shift of an image plane to neighboring PEs conditional, for each **PE** , upon a value stored in a mask register of each **PE** . A third technique, the carry propagate option, combines the computations from multiple PEs in order to complete an n-bit operation in fewer than n clocks by forming "supercells" within the array. The apparatus also includes a multi-bit X Pattern register and a multi-bit Y Pattern register. These registers have bit values corresponding to respective **columns** (for the X Pattern register) and rows (for the Y Pattern register) of the array. Patterns can be propagated from these registers into corresponding rows and **columns** . Further these registers can be used to receive values representing the logical OR of signals generated by individual PEs within respective rows and **columns** . Further, a number of global data registers are used to store information which can be broadcast back into the processing array.

French Abstract

L'invention concerne un dispositif de traitement de donnees possedant une architecture a instruction unique-donnees multiples (SIMD), et plusieurs fonctions ameliorant la performance et la facilite de programmation. Ce dispositif comprend une matrice rectangulaire de processeurs elementaires et un controleur. Il offre un certain nombre de techniques permettant de deplacer des donnees images dans la matrice. Une premiere technique, l'option "ROLL", deplace simultanement les plans image dans des directions opposees a l'interieur de la matrice. Une deuxieme technique, l'option de deplacement a porte, soumet le deplacement normal du plan image dans le PE adjacent a une condition definie pour chaque PE par une valeur memorisee dans un registre de motifs propre a chaque PE. Une troisieme technique, l'option de propagation-transport, combine les calculs d'une pluralite de PE afin de realiser une operation de n-bits en moins de n impulsions d'horloge par la formation de supercellules dans la matrice. Le dispositif comprend en outre un registre de motifs X multi-bits et un registre de motifs Y multi-bits. Ces registres ont des valeurs de bit correspondant aux colonnes respectives(pour le registre de motifs x) et aux rangees respectives (pour le registre de motifs y) de la matrice. Les motifs peuvent etre propages a partir de ces registres dans des rangees et des colonnes correspondantes. En outre ces registres peuvent etre utilise pour recevoir des valeurs representant le OU logique des signaux generes par les PE individuels dans les rangees et les colonnes respectives. Plusieurs registres de donnees globaux sont en outre utilises pour memoriser l'information qui peut etre rediffusee dans la matrice de traitement.

Main International Patent Class: **G06F-015/80**
Fulltext Availability:
Detailed Description

English Abstract

...shifting image data within the array. A first technique, the ROLL option, simultaneously shifts image planes in **opposite directions** within the array. A second technique, the gated shift option, makes a **normal** shift of an image plane to neighboring PEs conditional, for each **PE** , upon a value stored in a mask register of each **PE** . A third technique, the carry propagate option, combines the computations from multiple PEs in order to complete...

...Pattern register and a multi-bit Y Pattern register. These registers have bit values corresponding to respective **columns** (for the X Pattern register) and rows (for the Y Pattern register) of the array. Patterns

can be propagated from these registers into corresponding rows and **columns** . Further these registers can be used to receive values representing the logical OR of signals generated by individual PEs within respective rows and **columns** . Further, a number of global data registers are used to store information which can be broadcast back...

Detailed Description
... a rectangular PE array of whatever size is desired.

Device boundaries are invisible to the programmer for **normal** shift operations. For example, a shift to the east propagates thirty-two EO signals from the PEs 300 in the east-most **column** of one MCC 100 to the thirty-two El signals of the PEs 300 in the west-most **column** of the neighboring MCC to the east. These chip outputs are **bidirectional** , with a single signal pin being dedicated to each boundary **PE** 300, and as such, may impose some limitations which do not apply to the interior PEs 300 within the **PE** array 102. One limitation of the exemplary embodiment is that the boundary PEs 300 may communicate in...

28/5,K/34 (Item 34 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00522060 **Image available**
GLOBAL INPUT/OUTPUT SUPPORT FOR A MESH CONNECTED COMPUTER
SUPPORT GLOBAL D'ENTREE/SORTIE ORDINATEUR A ARCHITECTURE EN RESEAU
Patent Applicant/Assignee:
LOCKHEED MARTIN CORPORATION,
Inventor(s):
ABERCROMBIE Andrew P,
SUTHA Surachai,
HOLSZTYNSKI Wlodzimierz,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9953412 A1 19991021
Application: WO 99US7001 19990409 (PCT/WO US9907001)
Priority Application: US 9857468 19980409
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-015/80**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 12270

English Abstract
An apparatus for processing data has a Single-Instruction-Multiple-Data (SIMD) architecture, and a number of features that improve performance and programmability. The apparatus includes a rectangular array of processing elements and a controller. The apparatus offers a number of techniques for shifting image data within the array. A first technique, the ROLL option, simultaneously shifts image planes in **opposite directions** within the array. A second technique, the gated shift option, makes a **normal** shift of an image plane to neighboring PEs conditional, for each **PE** , upon a value stored in a pattern register of each **PE** . A third technique, the carry propagate option, combines the computations

from multiple PEs in order to complete an n-bit operation in fewer than n clocks by forming "supercells" within the array. The apparatus also includes a multi-bit X Pattern register and a multi-bit Y Pattern register. These registers have bit values corresponding to respective **columns** (for the X Pattern register) and rows (for the Y Pattern register) of the array. Patterns can be propagated from these registers into corresponding rows and **columns** . Further these registers can be used to receive values representing the logical OR of signals generated by individual PEs within respective rows and **columns** . Further, a number of global data registers are used to store information which can be broadcast back into the processing array.

French Abstract

L'invention concerne un dispositif de traitement de donnees possedant une architecture a instruction unique-donnees multiples (SIMD), et plusieurs fonctions ameliorant la performance et la facilite de programmation. Ce dispositif comprend une matrice rectangulaire de processeurs elementaires et un controleur. Il offre un certain nombre de techniques permettant de deplacer des donnees images dans la matrice. Une premiere technique, l'option "ROLL", deplace simultanement les plans image dans des directions opposees a l'interieur de la matrice. Une deuxieme technique, l'option de deplacement a porte, soumet le deplacement normal du plan image dans le PE adjacent a une condition definie pour chaque PE par une valeur memorisee dans un registre de motifs propre a chaque PE. Une troisieme technique, l'option de propagation-transport, combine les calculs d'une pluralite de PE afin de realiser une operation de n-bits en moins de n impulsions d'horloge par la formation de supercellules dans la matrice. Le dispositif comprend en outre un registre de motifs X multi-bits et un registre de motifs Y multi-bits. Ces registres ont des valeurs de bit correspondant aux colonnes respectives(pour le registre de motifs x) et aux rangees respectives (pour le registre de motifs y) de la matrice. Les motifs peuvent etre propages a partir de ces registres dans des rangees et des colonnes correspondantes. En outre ces registres peuvent etre utilise pour recevoir des valeurs representant le OU logique des signaux generes par les PE individuels dans les rangees et les colonnes respectives. Plusieurs registres de donnees globaux sont en outre utilises pour memoriser l'information qui peut etre rediffusee dans la matrice de traitement.

Main International Patent Class: **G06F-015/80**
Fulltext Availability:
Detailed Description

English Abstract

...shifting image data within the array. A first technique, the ROLL option, simultaneously shifts image planes in **opposite directions** within the array. A second technique, the gated shift option, makes a **normal** shift of an image plane to neighboring PEs conditional, for each **PE** , upon a value stored in a pattern register of each **PE** . A third technique, the carry propagate option, combines the computations from multiple PEs in order to complete...

...Pattern register and a multi-bit Y Pattern register. These registers have bit values corresponding to respective **columns** (for the X Pattern register) and rows (for the Y Pattern register) of the array. Patterns can be propagated from these registers into corresponding rows and **columns** . Further these registers can be used to receive values representing the logical OR of signals generated by individual PEs within respective rows and **columns** . Further, a number of global data registers are used to store information which can be broadcast back...

Detailed Description
... a rectangular PE array of whatever size is desired.

Device boundaries are invisible to the programmer for **normal** shift operations. For example, a shift to the east propagates thirty-two EO signals from the PEs 300 in the east-most **column** of one MCC 100 to the thirty-two El signals of the PEs 300 in the west-most **column** of the neighboring MCC to the east. These chip outputs are **bidirectional** , with a single signal pin being dedicated to each boundary **PE** 300, and as such, may impose some limitations which do not apply to the interior PEs 300 within the **PE** array 102. One limitation of the exemplary embodiment is that the boundary PEs 300 may communicate in...

28/5,K/35 (Item 35 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00522059 **Image available**
MESH CONNECTED COMPUTER
ORDINATEUR A ARCHITECTURE EN RESEAU MAILLE
Patent Applicant/Assignee:
LOCKHEED MARTIN CORPORATION,
Inventor(s):
ABERCROMBIE Andrew P,
DUNCAN David A,
MEEKER Woodrow L,
SCHOOMAKER Ronald W,
VAN DYKE-LEWIS Michele D,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9953411 A2 19991021
Application: WO 99US4299 19990409 (PCT/WO US9904299)
Priority Application: US 9857482 19980409
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-015/80**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 70382

English Abstract
An apparatus for processing data has a Single-Instruction-Multiple-Data (SIMD) architecture, and a number of features that improve performance and programmability. The apparatus includes a rectangular array of processing elements and a controller. In one aspect, each of the processing elements includes one or more addressable storage means and other elements arranged in a pipelined architecture. The controller includes means for receiving a high level instruction, and converting each instruction into a sequence of one or more processing element microinstructions for simultaneously controlling each stage of the processing element pipeline. In doing so, the controller detects and resolves a number of resource conflicts, and automatically generates instructions for registering image operands that are skewed with respect to one another in the processing element array. In another aspect, a

programmer references images via pointers to image descriptors that include the actual addresses of various bits of multi-bit data. Other features facilitate and speed up the movement of data into and out of the apparatus. "Hit" detection and histogram logic are also included.

French Abstract

La presente invention concerne un appareil de traitement de donnees qui presente une architecture SIMD (Single-Instruction-Multiple Data) et un certain nombre de caracteristiques qui en ameliorent les performances et la programmabilite. L'appareil comprend une matrice rectangulaire d'elements de traitement et un controleur. Selon un aspect de cette invention, chacun des elements de traitement comprend un ou plusieurs moyens de memoire adressables agences selon une architecture pipeline. Le controleur est dote de moyens permettant de recevoir des instructions de haut niveau et de convertir chacune de ces instructions en une sequence d'une ou de plusieurs micro-instructions pour element de traitement afin de commander simultanement chaque phase du pipeline d'elements de traitement. Grace a cette operation, le controleur detecte et resout un certain nombre de conflits d'acces aux ressources et genere automatiquement des instructions pour l'enregistrement d'operandes image qui sont decalees les uns par rapport aux autres dans la matrice d'elements de traitement. Selon un autre aspect de l'invention, un programmeur designe, via des pointeurs, des images renvoyant a des descripteurs d'image qui renferment les adresses effectives de divers bits de donnees multibits. D'autres caracteristiques facilitent et accelerent le mouvement de donnees qui entrent dans l'appareil et en sortent. L'invention comprend egalement un moyen de detection des existants de recherche et un histogramme logique.

Main International Patent Class: **G06F-015/80**
Fulltext Availability:
Detailed Description

Detailed Description
... a rectangular PE array of whatever size is desired. Device boundaries are invisible to the programmer for **normal** shift operations. For example, a shift to the east propagates thirty-two EO signals from the PEs...

...the west-most column of the neighboring MCC IC 101 to the east. These chip outputs are **bi - directional** , with a single signal pin being dedicated to each boundary **PE** 701, and as such impose some limitations which do not apply to the interior PEs 701 within the **PE** array 103. One limitation is that the boundary PEs 701 may communicate in one direction only during...
...function (described below), making operation of the ROLL position dependent. A second limitation is that shifts in **opposite directions** may not occur on consecutive clocks because the drivers need time to switch. This limitation affects all...

28/5,K/36 (Item 36 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00488455 **Image available**
METHODS AND APPARATUS FOR MANIFOLD ARRAY PROCESSING
PROCEDES ET APPAREIL DE TRAITEMENT MATRICIEL MULTIPLE
Patent Applicant/Assignee:
BOPS INCORPORATED,
Inventor(s):

PECHANEK Gerald G,
PITSIANIS Nikos P,
BARRY Edwin F,
DRABENSTOTT Thomas L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9919807 A1 19990422
Application: WO 98US21478 19981009 (PCT/WO US9821478)
Priority Application: US 97949122 19971010
Designated States: CA CN IL JP KR MX AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-015/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 17962

English Abstract
A manifold array topology includes processing elements, nodes, memories or the like arranged in clusters (52). Clusters are connected by cluster switch arrangements (986A) which advantageously allow changes of organization without physical rearrangement of processing elements. A significant reduction in the typical number of interconnections for preexisting arrays is also achieved. Fast, efficient and cost effective processing and communication result with the added benefit of ready scalability.

French Abstract
L'invention concerne une topologie de traitement matriciel multiple comprenant notamment des elements de traitement, des noeuds de traitement ou des memoires de travail repartis en groupes (52). Les groupes sont relies entre eux par des commutateurs de groupes (986A) permettant avantageusement de changer d'organisation, sans reagencement physique des elements de traitement. On arrive ainsi a reduire considerablement le nombre habituel d'interconnexions pour les matrices preexistantes. Un traitement et une communication rapides, efficaces et economiques aboutissent a une augmentation des disponibilites de reamenagement de la configuration.

Main International Patent Class: **G06F-015/00**
Fulltext Availability:
Detailed Description

Detailed Description
... hypercube connectivity.

A 5D hypercube 1900 is shown in Fig. 19, with 4 x 4 x 2 (**row** , **column** , plane) **PE** numbers shown as the top label in the PEs and the 5D hypercube numbers shown as the bottom **PE** number. For a conventional 5D hypercube, 5- **bidirectional** or 10-unidirectional connection ports are required in each **PE** . For the illustrated manifold array 2000 implementation shown in Fig. 20 in which a 5D hypercube is mapped onto a 4 x 4 x 2 manifold array, only 1 **bidirectional** or 2 unidirectional ports are required in each **PE** . In addition, the standard hypercube requires 2" or 32, PEs with a total of 5N2 (N=4) **bidirectional** buses or ION2(N=4) unidirectional buses. The 5D hypercube manifold array 2000 of Fig 20, requires only a total of 2N2(N=4) **bidirectional** buses or 4N2(N=4) unidirectional buses between all the clusters of PEs. Fig, 20 shows the...

28/5,K/37 (Item 37 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00465484 **Image available**
GRAPHICAL USER INTERFACE SUPPORTING METHOD AND SYSTEM FOR REMOTE ORDER GENERATION OF OFFICE FURNITURE PRODUCTS
PROCEDE ET SYSTEME DE SUPPORT D'INTERFACE UTILISATEUR GRAPHIQUE SERVANT A GENERER A DISTANCE DES INSTRUCTIONS CONCERNANT DES PRODUITS COMPLEXES DE MOBILIER DE BUREAU

Patent Applicant/Assignee:
HAWORTH INC,
SMITH Ward W,
ELLIS John M,
McNUTT Michael P,
SCHOEPPE Renee E,
Inventor(s):
SMITH Ward W,
ELLIS John M,
McNUTT Michael P,
SCHOEPPE Renee E,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9855949 A1 19981210
Application: WO 98US9890 19980520 (PCT/WO US9809890)
Priority Application: US 97870681 19970606
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-017/50**
International Patent Class: G06T-017/40; **G06F-017/60**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 14768

English Abstract
A graphical user interface to a method and system for configuring office furniture includes interface objects for obtaining configuration criteria from a user; presenting the user with at least one typical configuration satisfying the criteria; selecting a typical configuration from the at least one typical configuration; modifying aspects of the selected typical configuration to produce a modified configuration; and checking the validity of the modified configuration. The configuration criteria include conferencing criteria; privacy criteria; power criteria; communications criteria; storage criteria; and area criteria. A typical configuration can be modified by adding, deleting, or repositioning a component, changing the fabric or finish or the shape or size of the component. A cluster configuration based on the typical configuration is formed. The entire product line can be changed. At any time the entire typical or cluster configuration can be checked for validity and priced.

French Abstract
Interface utilisateur graphique concue pour un procede et pour un systeme servant a concevoir la configuration de mobilier de bureau a base d'objets d'interface servant a obtenir des criteres de configuration depuis un utilisateur. Ce procede consiste a presenter a l'utilisateur au moins une configuration typique repondant a ces criteres; a selectionner

une configuration typique particuliere; a modifier des aspects de la configuration typique selectionnee afin de produire une configuration modifiee; a verifier la validite de cette configuration modifiee. Ces criteres de configuration comprennent des criteres de conference, des criteres de confidentialite, des criteres de puissance, des criteres de communication, des criteres de rangement et des criteres de zone. On peut modifier une configuration typique par apport, suppression ou repositionnement d'un element, par modification du tissu, de la finition, de la forme ou de la dimension de l'element. On obtient une configuration groupee basee sur la configuration typique. On peut modifier la totalite de la ligne du produit. On peut a tout moment verifier la validite de la totalite de la configuration typique et groupee et en evaluer le prix.

Main International Patent Class: **G06F-017/50**
...International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
... Ighting C416 leither adjacent panel)
1-7T premise task light PR II"HML Prrn-til
premise **vertical storage** task light bracket PRIM I ???
places canopyjlght PLC IAttaches below places canopy
places counter top-@ask light...

...14)
Inherits Constraint
rod Line Properties C# Relationships L
nent Name J@P
!@a- 1ACCESSORY n
places **vertical storage** unit PLC rVa JACCESSORY.. n
gdd @@ n/a [ACCESSORY n
td mode-paper management bar PLC n...

28/5,K/38 (Item 38 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00442656 **Image available**
DISTRIBUTED AGREEMENT ON PROCESSOR MEMBERSHIP IN A MULTI-PROCESSOR SYSTEM
ACCORD DISTRIBUE CONCERNANT LE MAINTIEN DE PROCESSEURS DANS UN SYSTEME MULTIPROCESSEUR
Patent Applicant/Assignee:
TANDEM COMPUTERS INCORPORATED,
Inventor(s):
JARDINE Robert L,
BASAVAIAH Murali,
KRISHNAKUMAR Karoor S,
MURTHY Srinivasa D,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9833120 A1 19980730
Application: WO 98US1311 19980123 (PCT/WO US9801311)
Priority Application: US 97789257 19970128
Designated States: CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: **G06F-011/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 15632

English Abstract
A system to determine the group of processors that will survive communications faults and/or timed-event failures in a multi-processor system (100). The processors (112), each having a memory (118) and connected to an inter-processor communication network (114), detect that the set of processors with which they can communicate has changed. They then choose to halt or continue operations based on minimizing the likelihood that disconnected groups of processors will continue to operate as independent systems on the initiation of a regroup operation (622b). A processor is suspected of having failed when other processors detect the absence of a periodic message from the processor (682). When this happens, all of the processors are subjected to a series of stages in which they repeatedly broadcast their status and connectivity to each other (830). The suspected processor does not advance through the stages to regroup if it has ceased operations or if its timer mechanism has failed.

French Abstract
La presente invention concerne un systeme permettant de determiner le groupe de processeurs qui survivra a des defaillances de la communication et/ou a l'echec d'evenements programmes a intervalles precis dans un systeme multiprocesseur (100). Les processeurs (112) disposent chacun d'une memoire (118), et ils sont connectes au moyen d'un reseau (114) de communication inter-processeurs. Les processeurs detectent que l'ensemble de processeurs avec lesquels ils peuvent communiquer a change. Ils choisissent alors d'arreter ou de continuer leurs operations de maniere a minimiser la probabilite que les groupes de processeurs deconnectes continuent a fonctionner de facon independante. Lors du demarrage d'une operation de regroupement (622b). Un processeur est soupconne de souffrir d'une panne lorsque les autres processeurs detectent l'absence d'un message periodique devant etre transmis par ledit processeur (682). Lorsque cette situation se presente, tous les processeurs doivent passer par une serie d'etapes au cours desquelles ils se communiquent les uns aux autres a plusieurs reprises leur statut et leur connectivite (830). Le processeur soupconne ne peut pas avancer d'une etape a l'autre s'il a cesse ses operations ou si son mecanisme d'horloge est en panne.

Main International Patent Class: **G06F-011/00**
Fulltext Availability:
Claims

Claim
... C is in
canonical form if and only if:
(1) if a processor i is dead, the **row** C(i,x) is FALSE, and the **column** C(x,i) is FALSE; and
(2) if C(i,j) is FALSE, C(ji) is FALSE. This ensures symmetric or **bidirectional** connectivity.
- connected graph: a graph in which no processor is isolated from all other processors in the...

...vertices of the graphs are the processors, and the edges are the communication links. The edges are **bi - directional** .
The terms "vertex" and "processor" are used interchangeably, as are the terms "communication link," "link" and "edge...j) is set to TRUE if the processor i is communicatively connected to the processor i (i **pE** j). The entry C(i,j) is set to FALSE if the processor i is not communicatively...

28/5,K/39 (Item 39 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00303259 **Image available**
REPLICATOR SYSTEM AND METHOD FOR DIGITIZING THE GEOMETRY OF A PHYSICAL OBJECT
SYSTEME ET PROCEDE DE REPRODUCTION POUR NUMERISER LA GEOMETRIE D'UN OBJET PHYSIQUE
Patent Applicant/Assignee:
RADICAL ADVANCED TECHNOLOGIES CORP,
GUBELMANN Stephen,
Inventor(s):
GUBELMANN Stephen,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9521410 A1 19950810
Application: WO 94US1233 19940202 (PCT/WO US9401233)
Priority Application: WO 94US1233 19940202
Designated States: AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB GE HU JP KP KR KZ LK LU LV MG MN MW NL NO NZ PL PT RO RU SD SE SK UA US UZ VN AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: **G06F-003/14**
International Patent Class: **G06F-03:153** ; **G06F-15:46** ; G05B-19:02
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 19933

English Abstract
A system (100) and method for replicating the geometry of a physical object (122) includes a computer (102) and storage means (108) for storing data representative of features of a multidimensional object (122). The system (100) includes an input device (112) that is used for identifying locations in three-dimensional space, and for providing signals representative of those locations. Means (106) responsive to the input signals is provided to define a line in the system extending across at least a portion of space defined as containing the object (122). A user diverts the input device (112) to a location on the object (122) to intersect a portion of a cut plane which is defined on the line. This and other user input defined locations are retrieved and stored by the computer (102). When finished the collective defined locations are used to define the object (122) in three-dimensional space.

French Abstract
L'invention se rapporte a un systeme (100) et un procede de reproduction de la geometrie d'un objet physique (122), ce systeme comprenant un ordinateur (102) et un dispositif de stockage (108) pour stocker des donnees representant les caracteristiques d'un objet multidimensionnel (122). Le systeme (100) comprend un dispositif d'entree (112) qui est utilise pour identifier des emplacements dans l'espace tridimensionnel, et pour generer des signaux representant ces emplacements. Un dispositif (106) sensible aux signaux d'entree est prevu pour creer dans le systeme une ligne qui traverse au moins une partie de l'elpace defini comme contenant l'objet (122). Un utilisateur transfere le dispositif d'entree (112) vers un point sur l'objet (122), afin d'entrecroiser une partie d'un plan coupe qui est defini sur la ligne. Ce point et d'autres points definis par l'entree d'utilisateur sont extraits et stockes par

l'ordinateur (102). Lorsque cette operation est achevee, les points definis groupes sont utilises pour former l'objet (122) dans l'espace tridimensionnel.

Main International Patent Class: **G06F-003/14**
International Patent Class: **G06F-03:153** ...

... **G06F-15:46**
Fulltext Availability:
Detailed Description

Detailed Description
... 3 unique pts
ml = (Ipt2[l3-ptl[13)/(pt2EO]-ptIE03)
ne = (Pt3IlI-pt2El1)/(pt3E03-pt2[03)
/* construct **perpendicular** bisectors of the two tines with slopes ml, m2
pt4[O]=(ptlEOI+pt2[O])/2
pt4[11...

...t be used since slope will be infinite
b5 = pt5[13-m5*pt5L03
/* intersection of the two **perpendicular** bisectors is the arc center
/* first bisector must be **vertical** tine in new view */
/* centerI03 = 05-b4mm4-m5) remove due to divide by zero problems
center[01...

...0)
an92 = acos(reLx3/rad)
else
ang2 = 360 - acos(reLx3/rad)
:doit
CLS -1
redraw -1
Mode **normal**
arc center(Ol. centerI13, center[21, rad, angl, ang2, sysview
LastEnt=@Lastid
if (Points)
for 0=0...

...O],Origin[13,origin[21,BLack
nderID= lastid
else
auto -1
redraw -1
goto start
:exit
Mode **normal**
clear PntNodes.PntIDs.ptl, pt2, pt3, pt4j pt5, center, vmx
if (Finder)
DELENT FinderlD
EXIT
SUBSTITUTE: SHEET...DELENT SpLnEnt[l]
SptnEnt[OJ=SpLnEnt[l1=O
on Spiane goto XY,XZ,YZ
Sdptane=O
:Oti: **pe** =xoit
:XY
ARRAY PLnDeflE41E33
PLnDefl [01 [03=PInDefl 133 CO =Or!gin[01+(GridSize*-l)
PlnDefl El...

28/5,K/40 (Item 40 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00234265 **Image available**
SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE DECISION

Patent Applicant/Assignee:
STAR SEMICONDUCTOR CORPORATION,
Inventor(s):
ROBINSON Jeffrey I,
ROUSE Keith,
KRASSOWSKI Andrew J,
MONTLICK Terry F,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9308524 A1 19930429
Application: WO 92US8954 19921014 (PCT/WO US9208954)
Priority Application: US 91776161 19911015
Designated States: AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Main International Patent Class: **G06F-009/00**
International Patent Class: **G06F-09:40**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 219172

English Abstract
Architectures and methods are provided for efficiently dividing a processing task into tasks for a programmable real time signal processor (SPROC) (10) and tasks for a decision-making microprocessor (2120). The SPROC is provided with a non-interrupt structure where data flow is through a multiported central memory. The SPROC is also programmed in an environment which requires nothing more than graphic entry of a block diagram of the user's design. In automatically implementing the block diagram into silicon, the SPROC programming/development environment accounts for and provides software connection and interfaces with a host microprocessor (2120). The programming environment preferably includes: a high-level computer screen entry system which permits choosing, entry, parameterization, and connection of a plurality of functional blocks; a functional block cell library (2015) which provides source code representing the functional blocks; and a signal processor scheduler/compiler (2040) which uses the functional block cell library (2015) and the information entered into the high-level entry system to compile a program and to output source program code for a program memory and source data code for the data memory of the SPROC, as well as a symbol table which provides a memory map which maps SPROC addresses to variable names which the microprocessor (2120) will refer to in separately compiling its program.

French Abstract
On decrit des architectures et procedes qui permettent de separer efficacement une tache de traitement en taches destinees a un processeur de signaux programmable fonctionnant en temps reel (SPROC)(10) et a un microprocesseur de prise de decision (2120). Le SPROC est dote d'une structure depourvue d'interruption ou le flux de donnees arrive par

l'intermediaire d'une memoire centrale a ports multiples. Il est aussi programme dans un environnement n'exigeant rien d'autre que l'introduction graphique d'un schema global relatif aux intentions de l'utilisateur. Avec la realisation automatique du schema global dans le silicium, l'environnement de programmation et de developpement du SPROC prend en compte et fournit la connexion au logiciel et realise une interface avec un microprocesseur hote (2120). Cet environnement de programmation comporte de preference un systeme d'introduction a ecran d'affichage perfectionne qui permet de choisir, introduire, parametriser et fournit une connexion avec differents blocs fonctionnels; une bibliotheque a cellules de bloc fonctionnel (2015) qui fournit un code source representant les blocs fonctionnels; et un programmateur/compileur pour processeur de signal (2040). Ce dernier utilise la bibliotheque a cellules (2015) et l'information introduite dans le systeme d'introduction perfectionne pour compiler un programme et delivrer en sortie un code de programme source concernant une memoire du programme et un code de donnees source destine a la memoire de donnees du SPROC, ainsi qu'une table de symboles qu fournit une cartographie memorisee, contenant les adresses donnees par le SPROC aux differents noms auxquels le microprocesseur (2120) viendra se referer en compilant separement son propre programme.

Main International Patent Class: **G06F-009/00**
International Patent Class: **G06F-09:40**
Fulltext Availability:
Claims

Claim
... the value in the base or frame register (i.e. the "B indexed mode" or T indexed **mode** ") in order to generate an address, muxBF 487 selects appropriately the Breg 476 or the Freg 477...n %s", Loa-rec); /* always print it:
return (i
FUNCTION DEFINITION: row not sent
see if current **row** (string) in an array exists earlier in the array, return 0 if current entry does not exist...1.1 1991/08/13 13:56:24 allsop
Initial revision
source.sdl
Function:
This routine reads **consecutive** inputs from a file (array) of specified length, and outputs them, one at a time. The array...infa);
free(item->name-str);
free(item);
end of free-node
#andif
void free List(node t **pe** *List)
y
node-type *work, *temp;
/* traverse List freeing as we go... *1
while (work) C
temp...

28/5,K/41 (Item 41 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00207472 **Image available**
IMPROVED MEMORY SYSTEM
SYSTEME DE MEMOIRE AMELIORE
Patent Applicant/Assignee:

HYATT Gilbert P,
Inventor(s):
HYATT Gilbert P,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9204673 A1 19920319
Application: WO 91US6285 19910903 (PCT/WO US9106285)
Priority Application: US 9041 19900904
Designated States: AT BE CA CH DE DK ES FR GB GR IT JP KR LU NL SE
Main International Patent Class: **G06F-012/02**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 137004

English Abstract
Memory technologies for storing include RAMS and CCDs. Adaptive memory capability and memory servo capability improve memory characteristics. In a RAM embodiment, a detector (220B, 220A) is used to detect a memory address condition (217) and to control the memory (222) and the memory address register (218) in response thereto. In a CCD embodiment, a detector (220A, 220B) is used to detect a memory reference signal (217) and to refresh the memory signals (221A, 221B, 221) in response thereto. Improved memory refresh, memory performance, and memory capacity enhance system characteristics. Improved memory architecture provides advantages of increased speed, lower cost, and efficiency of implementation. Information stored in memory can be scanned out at a rate greater than the addressing rate associated with the memories. This permits higher speed operation with lower cost memories. Use of an output buffer, such as a FIFO, permits normalization of memory clock rates.

French Abstract
Les technologies de stockage en memoire comprennent des memoires vives et des dispositifs a couplage de charge. La fonction memoire adaptative et la fonction servomemoire ameliorent les caracteristiques de memoire. Dans un mode de realisation de memoire vive, on utilise un detecteur (220B, 220A) afin de detecter un etat d'adresse en memoire (217) et afin de commander la memoire (222) ainsi que le registre d'adresses en memoire (218) en reponse audit etat. Dans un mode de realisation de dispositif a couplage de charge, on utilise un detecteur (220A, 220B) afin de detecter un signal de reference de memoire (217) et afin de regenerer les signaux memoire (221A, 221B, 221) en reponse a ce dernier. La regeneration, les performances et la capacite ameliorees de la memoire ameliorent les caracteristiques du systeme. Une architecture de memoire amelioree offre les avantages d'une vitesse accrue, d'un cout inferieur et d'une efficacite de mise en oeuvre. Les informations stockees en memoire peuvent etre parcourues et extraites a une vitesse superieure a la vitesse d'adressage associee aux memoires. Cet agencement permet un fonctionnement a vitesse superieure avec des memoires de cout inferieur. L'emploi d'un tampon de sortie tel qu'un systeme premier entre premier sorti (FIFO), permet la normalisation de frequences de base de memoire.

Main International Patent Class: **G06F-012/02**
Fulltext Availability:
Detailed Description

Detailed Description
... memory on an online basis time shared with refreshing of the display on an online basis.

One **arrangement** of the graphics system of the present invention is

shown in
Fig 1. Supervisory processor 115A loads...vector memory can be performed in a manner similar to loading the address generators from the supervisory **processor** , as shown in the LD.ASC program listing herein and as discussed relative to the supervisory processor...address register with memory will now be discussed for a special purpose processor; such as a display **processor** , **array** processor, filter processor, signal processor, cache memory processor., artificial intelligence processor, or other application. A memory address...sync pulse, the leading portion of a line sync pulse in this illustration.

SUBSTITUTE SHEET
-102
The **vertical** sync memory refresh detector circuits and the line sync memorv refresh detector circuits are discussed here for...AND CLSRI AND CLSR4)
2o The RUN signal covers the period of time when the CFSR1 signal (**vertical** sync pulse) is low and either the line sync pulse is low CLSR1 * or the trailing portion...

28/5,K/42 (Item 42 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00192848
SCALABLE INTER-PROCESSOR AND PROCESSOR TO I/O MESSAGING SYSTEM FOR PARALLEL PROCESSING ARRAYS
SYSTEME DE MESSAGERIE EVOLUTIF INTERPROCESSEUR ET PROCESSEUR VERS E/S POUR RESEAUX DE TRAITEMENT PARALLELE
Patent Applicant/Assignee:
MASPAR COMPUTER CORPORATION,
Inventor(s):
NICKOLLS John R,
ZAPISEK John,
KIM Won S,
KALB Jeffrey C,
BLANK W Thomas,
WEGBREIT Eliot,
VAN HORN Kevin,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9110197 A1 19910711
Application: WO 91US77 19910104 (PCT/WO US9100077)
Priority Application: US 90492 19900105
Designated States: AT AU BE CA CH DE DK ES FR GB GR IT JP LU NL SE SU
Main International Patent Class: **G06F-015/00**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 42225

English Abstract
A massively parallel computer system (500) is disclosed having a global router network in which pipeline registers are spatially distributed to increase the messaging speed of the global router network. The global router network includes an expansion tap for processor to I/O (1700) messaging so that I/O messaging bandwidth matches interprocessor messaging bandwidth. A route-opening message packet includes protocol bits which are treated homogeneously with steering bits. The route-opening packet further includes redundant address bits for

imparting a multiple-crossbars personality to router chips within the global router network. A structure and method for spatially supporting the processors (700) of the massively parallel system and the global router network are also disclosed.

French Abstract

Systeme informatique (500) parallele sur une grande echelle, comportant un reseau d'acheminement global dans lequel des registres pipeline sont repartis dans l'espace afin d'augmenter la vitesse de transmission de message du reseau d'acheminement global. Le reseau d'acheminement global comprend un branchement d'expansion permettant la messagerie processeur a E/S (1700), de sorte que la largeur de bande de messagerie E/S s'adapte a la largeur de bande de messagerie interprocesseur. Un paquet de message d'ouverture d'itineraire comprend des bits de protocole, lesquels sont traites de maniere homogene a l'aide de bits de direction. Le paquet d'ouverture d'itineraire comprend egalement des bits d'adresses redondants, destines a conferer une personnalite a barres croisees multiples a des puces d'acheminement situees a l'interieur du reseau d'acheminement global. L'invention concerne egalement une structure et un procede de soutien dans l'espace des processeurs (700) du systeme parallele a grande echelle, et du reseau d'acheminement global.

Main International Patent Class: **G06F-015/00**
Fulltext Availability:
Detailed Description

Detailed Description
... processor element, PEx,1 has a message originating wire 410x coupled to a first terminal of a **bidirectional** pipeline latch, i.e., 415x within the first stage latch set 415. The suffix x denotes here a 30 corresponding one of the suffixes for identifying individual processor elements **PE** ,, **PE** @,, PE3,, etc. in an array AN, individual wires 410a, 410b, 410c, etc. in an array-to-stage...

...426b, 426c, etc. in a latch-to switch-matrix connecting bus 416. A second terminal of each **bidirectional** register 415x is coupled to a first stage **horizontally** -extending wire 462x passing from the connecting bus 416 into first **bidirectional** switching stage 460A. Although arrowheads are shown on the wires 410x, 462x and others in Figure 4A, it is to be understood 5that the message routing paths.formed by these wires are **bidirectional** and that the arrows are included merely for the sake of simplifying the explanation of a left...

...PEx to the target processor PEy or the other way through the opened path , from PEY to **PE** ., a Within the first NXM (i,e., 16x4) switching stage 460A. there is provided a number M (i*e,j M=4) of first 15 stage **vertical** wires 464 extending to overlap the N first stage **horizontal** wires 462. Switching elements 463 are provided at the intersections of the first-stage **horizontal** and **vertical** wires, 462 and 464, for selectively routing a message (either unidirectionally or 20 **bidirectionally**) through a predetermined one of the first stage **horizontally** extending wires 462 and from there, on to a header-selected one of the first stage **vertically** extending wires 464,

As in the crossbar "wormholing" technique of Fig* 3Bj, in Figure 4A a route...

...sends a first route-requesting field of bits (B of full header BFI) onto the first stage **horizontal** wire 462c. A corresponding switch element 463 in **horizontal** set 463cA, 463cB, 463cC and 463cD closes to thereby "retire" the first field, B of Header = BF1...

...field with movement of the remaining request-bits (F1 of Header = BFI) onto a distinguishable one of **vertical** wires 464A, 464B, 464C and 464D.
In Fig. 4A. each first stage vertical wire 464Y (Y denotes...one of the four wires of wire group WG-A* to a corresponding one of the four **horizontal** wires,472a 5472a-2, 472a-3 and 472a-4 of substage 46OBa*. Similarly, each of function boxes 425b*, 425c* and 425d* represents a IF plurality of H **bidirectional** pipeline registers coupling the individual wires 465x* of their respective wire groups WG-Y* to the corresponding...

...stored in the first pipeline latch 415c for one bit period apiece and then forwarded along first **horizontally** extending line 462c into the first (hyperbar) switching stage 460A*. Hyperbar stage 460A* opportunistically grants to the requesting processor, PE31 25 whichever one of the H **vertical** output wires 464B* in wire-group WG@B*, that is next available. Here, we will assume that one of other processor elements **PE** , or PE2 has already grabbed **vertical** wire 464B, and that **vertical** wire 464B. is the next wire available to be granted to PE3 from 30 among the wires...to 10 the "reverse" mode so that the acknowledge signal (ACK) may be sent back through the **bidirectional** router network from each recipient device (i.e., PER or IOER) whose R-register had been set...Since the last bit, n+3, of the forward MEND packet 552 cannot reach the intended target (**PE** @ or IOFrr) until 4 bit times after being launched into the router 560 (because of the time...

...until a bit time of approximately n+9 or thereafter. The receiving 30 devices (PER or IOER) **normally** need a number of bit times to evaluate the received address bits Co, C1, RO, R1 and...

...Yz) of the stage-3 router chip 600,, passes through reverse driver 656, moves down the corresponding **vertical** wire 641@644, through the closed route-granting switch GSW(Yz) of the originating **row** x, 10 through the **horizontal** message-data carrying wire 650x, and from there, into the front end circuitry 610x, wherein the acknowledge...

...same reverse path through the stage-2 and stage-1 router chips 600. When the message-originating **PE** , processor receives 20 the acknowledge signal (i.e. the TB, PB = 01 stream), the message originating processor...

...to the target processor PET (or 1/0 device IOET) a At that point, the

originating device **PE** , shuts off a transmit-request flag 25 set in its local T-register 728 (see Fig. 7A)o If no acknowledge signal (ACK) is sent back to the message originating processor **PE** ., then the message@originating processor sees all lows (000 **a 0) indicating ...90 657x weakly to low in cases where no granting switch GSW(x,Yz) has closed in **row** -x and thus the originating **PE** will receive a constant 00 as a non-acknowledge signal during the RCLOSE operation instead of the...

28/5,K/43 (Item 43 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00154839
APPARATUS FOR ENHANCING AND THRESHOLDING SCANNED MICROFILM IMAGES AND METHODS FOR USE THEREIN
APPAREIL PERMETTANT L'AMELIORATION ET LA DETERMINATION DU SEUIL D'IMAGES MICROFILMEES EXPLOREES, ET SES PROCEDES D'UTILISATION
Patent Applicant/Assignee:
EASTMAN KODAK COMPANY,
Inventor(s):
MORTON Roger Roy Adams,
REDDEN John Edward,
LEWIS Scott,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8901205 A1 19890209
Application: WO 88US2348 19880714 (PCT/WO US8802348)
Priority Application: US 87529 19870724
Designated States: AT BE CH DE FR GB IT JP NL SE
Main International Patent Class: **G06F-015/68**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 30892

English Abstract
Apparatus for enhancing and thresholding scanned microfilm images, specifically for removing single pixel noise therefrom, and accompanying methods for use therein are disclosed. Specifically, this apparatus convolves each one of a pre-defined group of incoming pixel values with a corresponding one of a pre-defined set of coefficients in order to generate a convolved pixel value. The convolved pixel is then compared against a threshold level to produce a thresholded pixel value indicative of the results of the comparison. The inventive apparatus also includes a noise processing circuit that contains a noise tracker and a noise detector and filter circuit. The noise tracker is used to produce a noise value that tracks a noise level present in the thresholded pixel value. The noise detector and filter circuit filters pixel noise from the thresholded pixel value and, in response thereto, produces a corresponding output pixel value for a current incoming pixel value being processed and provides a signal to the noise tracker that pixel noise has been detected. A background tracker, which also forms part of the inventive apparatus, produces a background value that tracks a background level present in the incoming pixel values. The background value and the noise value are combined to produce an error signal which, in turn, is used, along with a deaveraged value of the current incoming pixel value, to set the threshold level for the current pixel value being processed. Specific apparatus for the background tracker and noise tracker, and

accompanying methods for use therein, are also disclosed herein.

French Abstract

Appareil permettant l'amelioration et la determination du seuil d'images microfilmees explorees, specifiquement destine a en eliminer le bruit de pixel unique, et ses procedes d'utilisation. Plus precisement, cet appareil convolutionne chaque valeur d'un groupe predefini de valeurs de pixel entrant, avec un coefficient d'un ensemble pre-defini de coefficients afin de produire une valeur de pixel convolutionne. On compare ensuite le pixel convolutionne a un niveau de seuil afin de produire une valeur de pixel a seuil determine indiquant les resultats de la comparaison. L'appareil de l'invention comprend egalement un circuit de traitement de bruit comportant un dispositif suiveur de bruit, un circuit detectant et filtrant le bruit. Le dispositif suiveur de bruit sert a produire une valeur de bruit suivant un niveau de bruit present dans la valeur de pixel a seuil determine. Le circuit detectant et filtrant le bruit filtre le bruit de pixel a partir de la valeur de pixel a seuil determine et, en reponse a celle-ci, produit une valeur de pixel de sortie correspondante, destinee a une valeur de pixel entrant actuelle en cours de traitement, et transmet un signal au dispositif suiveur de bruit dont le bruit de pixel a ete detecte. Un dispositif suiveur de fond, faisant egalement partie de l'appareil de l'invention, produit une valeur de fond suivant un niveau de fond present dans les valeurs de pixel entrant. On combine la valeur de fond et la valeur de bruit afin de produire un signal d'erreur qui, a son tour, est utilise, avec une valeur hors moyenne de la valeur de pixel entrant actuelle, afin d'etablir le niveau de seuil pour la valeur de pixel en vigueur, en cours de traitement. Des appareils specifiques destines au dispositif suiveur de fond et au dispositif suiveur de bruit, ainsi que leurs procedes d'utilisation sont egalement decrits.

Main International Patent Class: **G06F-015/68**
Fulltext Availability:
Detailed Description

Detailed Description
... film which, in turn, enters optical system 20. The optical system ensures that light for only one **horizontal** scanning line, typically that lying between rays 14 and 16 inclusive, reaches CCD array 22, In practice, optical system 20 is set to overscan each **horizontal** scanning line that constitutes image 11 by approximately 50%. By doing so, the full image will be...

...somewhat off center or tilted (as shown in FIG. 1) and/or if the CCD becomes slightly **horizontally** mis-aligned with respect to the microfilm, Overscanning is necessary particularly where rotary microfilmers have been used...

...Once the current line has been scanned, the film transport mechanism (not shown) in the film library **vertically** 5 advances the film in the direction of arrow 9 to appropriately bring the next image of...

...document into a proper starting position behind optical system 20, Once this occurs, CCD array 22 moves

vertically through the image one scan line at a time. Lamp 7 is appropriately energized, via lamp driver...

...situated within image processing circuit 40, CCD array 22 typically consists of two interlaced groups of 1024 **serially connected** CCD cells: one group for the odd pixels and the other group for the even pixels. Under...

28/5,K/44 (Item 44 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2002 WIPO/Univentio. All rts. reserv.

00106554 **Image available**
DATA PROCESSING SYSTEM
SYSTEME DE TRAITEMENT DE DONNEES
Patent Applicant/Assignee:
INTEL CORP,
Inventor(s):
COLLEY S,
RATTNER J,
COX G,
SWANSON R,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8102477 A1 19810903
Application: WO 80US205 19800228 (PCT/WO US8000205)
Priority Application: WO 80US205 19800228
Designated States: DE GB JP AT CH DE FR GB LU NL SE
Main International Patent Class: **G06F-003/00**
International Patent Class: **G06F-07:00** ; **G06F-09:00** ; **G06F-13:00** ; **G06F-15:16** ; **G06F-15:20**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 139912

English Abstract
A data processor architecture wherein the processors recognize two basic types of objects, an object being a representation of related information maintained in a contiguously addressed set of memory locations. The first type of object contains ordinary data, such as characters, integers, reals, etc. The second type of object contains a list of access descriptors. Each access descriptor provides information for locating and defining the extent of access to an object associated with that access descriptor. The processors recognize complex objects that are combinations of objects of the basic types. One such complex object (94) defines an environment (18 or 20) for execution of objects (92, 93, 98, 106, 122) accessible to a given instance of a procedural operation. The dispatching of tasks to the processor is accomplished by hardware-controlled queuing mechanisms (36), dispatching-port objects (146) which allow multiple sets of processors (38) and (40) to serve multiple, but independent sets of tasks (14, 16). Communication between asychronous tasks or processes is accomplished by related hardware controlled queuing mechanisms (34) (buffered-port objects) (144) which allow messages to move between internal processes or input/output processes without the need for interrupts. A mechanism (42) is provided which allows the processors to communicate with each other. This

mechanism is used to reawaken an idle processor to alert the processor to the fact that a ready-to-run process at a dispatching port needs execution.

French Abstract

Structure de processeur de donnees dans laquelle les processeurs reconnaissent deux types fondamentaux d'objets, un objet etant constitue par une representation d'informations connexes maintenues dans un groupe d'emplacements de memoire adresse en contiguite. Le premier type d'objets contient des donnees ordinaires, telles que des caracteres, des nombres entiers, reels, etc. Le deuxieme type d'objets contient une liste de descripteurs d'acces. Chaque descripteur d'acces fournit une information servant a localiser et definir l'etendue de l'acces a un objet associe a ce descripteur. Les processeurs reconnaissent des objets complexes constitues par des combinaisons d'objets des types fondamentaux. Un tel objet complexe (94) definit un environnement (18) ou (20) pour l'execution d'objets (92, 93, 98, 106, 122) accessible a un moment donne d'une operation de traitement. La repartition des taches aux processeurs est executee par des mecanismes (36) de mise en file d'attente commandes par le materiel, des objets (146) de points de connexion de repartition permettant a des groupes multiples de processeurs (38 et 40) d'executer des ensembles de taches (14, 16) multiples mais independantes. La communication entre des taches ou traitement asynchrones est executee par les mecanismes (34) relatifs de mise en file d'attente commandes par le materiel (objets de points de connexion dotes d'un tampon) (144) permettant la circulation des messages entre les traitements internes ou les operations d'entree/sortie sans que des interruptions soient necessaires. Un mecanisme (42) est prevu permettant la communication entre les processeurs. Ce mecanisme est utilise pour reactiver un processeur inactif pour signaler au processeur une operation prete a passer a un point de connexion de repartition avant d'etre executee.

Main International Patent Class: **G06F-003/00**
International Patent Class: **G06F-07:00** ...

... **G06F-09:00** ...

... **G06F-13:00** ...

... **G06F-15:16** ...

... **G06F-15:20**
Fulltext Availability:
Detailed Description

Detailed Description
... system linkage objects called nonbuffered communication ports (104, FIGURE 3A).. Conceptually, a nonbuffe 'red port contains a **single** entry.

They are represented by a single-entry access list, 105, as shown in FIGURE 3.

When...for service
111 - waiting for maintenance
The interpretation of the trace mode subfield is as follows.

00 - **normal mode**
01 - fault trace mode
10 - flow trace mode
11 - full trace mode

The clock-mode bit indicates...qualify processor object
qualify segment table directory
nitialize segment table directory
90
enter alarm mode
enter -diagnostic **mode**
enter **normal** **mode**
diagnose
stop
dequeue
suspend for diagnosis
uspend normally
count value in a processor control segment will be...enter the unassigned state. SUSPEND NORMALLY implies STOP after suspension is complete if there are no other **processor** -control flags set, For a processor which is not currently serving a process, no response is required...

Search report

Set	Items	Description
S1	103	MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCESSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGEMENT? OR ORDER OR FORMATION)
S2	113	(SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N)(CONNECT? OR LINK?) OR SINGLE()BIT
S3	24	MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?)
S4	30	MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5	21	MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6	0	VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7	1510	VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8	1003	HORIZONTAL? OR ROW OR NORMAL?
S9	297	BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE
S10	216	S1 OR S2
S11	0	S10 AND S3 AND S4
S12	1	S10 AND S3
S13	0	S10 AND S4
S14	0	S10 AND S5
S15	0	S10 AND S7 AND S8 AND S9
S16	8	S10 AND S7
S17	4	S10 AND S8
S18	1	S10 AND S9
S19	11	S12 OR S16 OR S17 OR S18
S20	11	S19 NOT PY>2000
S21	11	S20 NOT PD>20000831

File 256:SoftBase:Reviews,Companies&Prods. 82-2002/Jul
(c)2002 Info.Sources Inc

21/5/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

01544183 DOCUMENT TYPE: Product

PRODUCT NAME: ANZIO (544183)

Rasmussen Software Inc (592153)
10240 SW Nimbus Ave #L9
Portland, OR 97223 United States
TELEPHONE: (503) 624-0360

RECORD TYPE: Directory

CONTACT: Sales Department

ANZIO is a family of products that offer thorough, reliable and easy-to-use terminal super-emulation between PCs and host systems running any veriant of UNIX. A full range of file transfer capabilities is also available. Super-emulation means these products go way beyond simply emulating a dumb terminal. They provide support for macro keys, user comfort features, keystroke compatibility, pass-through print and 132- **column mode** . When users run any of the programs, their PC becomes a terminal on a host system. Users can then run any host-based program using a dumb terminal. Specifically these products emulate many common terminal types including VT220/ANSI, Wyse 60, ADDS Viewpoint and Verssys C332. The system supports all versions of Windows, DOS and both TCP/IP and **serial connections** . All the products in the family are software only.

DESCRIPTORS: Terminal Emulators; Data Communications

HARDWARE: IBM PC & Compatibles
OPERATING SYSTEM: MS-DOS; Windows; Windows NT/2000
PROGRAM LANGUAGES: Not Available
TYPE OF PRODUCT: Micro
DATE OF RELEASE: 01/83
PRICE: Available upon request; varies by product; demo disk available

DOCUMENTATION AVAILABLE: User manuals
TRAINING AVAILABLE: Technical support
REVISION DATE: 020410

21/5/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

01240699 DOCUMENT TYPE: Product

PRODUCT NAME: ICE.TEN (240699)

J River Inc (327263)
211 N 1st St #375
Minneapolis, MN 55401 United States
TELEPHONE: (612) 677-8200

RECORD TYPE: Directory

CONTACT: Sales Department

ICE.TEN is the serial version of ICE. Using **serial** lines to **connect** PCs to UNIX, it supports baud rates to 115,200. The system provides complete terminal emulation yet requires little memory. Windows versions of terminal emulation, file transfer, printing and setup programs are included. It emulates SCO ANSI Color Console, AT&T605, VT102, VT220, IBM3151, AT386 ANSI Color Console, Wyse60 and Wyse160 including WordPerfect View and fax document preview. Features include: (1) 132- **column** by 43-line displays, color and escape sequence features; (2) multiple sessions are available when used with a UNIX multi-session program; (3) file transfer program which uses a familiar Windows point-and-click interface; (4) support for Zmodem as well as **normal** and quoted Xmodem and Ymodem (Zmodem and quoted protocols provide higher reliability for transfers using terminal servers or modems); (5) Host Print which permits Windows applications to print transparently to any UNIX printer and also intercepts and reroutes print jobs (text or graphics) from LPT1, LPT2 and LPT3; (6) terminal emulations support Local Print allowing users to print from a UNIX application to a printer connected to the parallel port of a PC; (7) the configuration program lets users change terminal emulation, program keys, map characters and set up printing; and (8) support for international character sets and keyboards.

DESCRIPTORS: Terminal Emulators; File Transfer; Telecommunications; Data Communications

HARDWARE: IBM PC & Compatibles
OPERATING SYSTEM: Windows; Windows NT/2000; UNIX
PROGRAM LANGUAGES: Not Available
TYPE OF PRODUCT: Micro; Workstation
POTENTIAL USERS: Cross Industry
PRICE: Available upon request
REVISION DATE: 001012

21/5/3
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00110355 DOCUMENT TYPE: Review

PRODUCT NAMES: DB2 Universal Database 5 Windows NT (656852)

TITLE: Database Relations: SQL Server grande dame DB2 works to improve in...
AUTHOR: Winters, David
SOURCE: BackOffice Magazine, p52(6) Aug 1998
ISSN: 1084-6433

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: A

IBM's recommended DB2 Universal Database 5 on Windows NT is a universal database that provides replication, support for multiple CPUs, support for Windows 95 and Windows 98, **row** -level locking, parallel querying, parallel bulk copying, partition-based named object caches, support for the Web and BLOBs, an Open Database Connectivity (ODBC) interface, and some support for SQL 92. Testers found that the product ran like a Windows NT-customized package, performing extremely well for disk, memory, and CPU usage. DB2 also natively uses the Windows NT Event Log, and users are partly managed using the NT User Manager. The administrative server (DB2DAS00) is required to run comprehensive user administration features locally or remotely. The

interface is greatly improved, but is still awkward and immature. It is called the Control Center and has a metaphor similar to those of Microsoft SQL Enterprise Manager, Embarcadero DBArtisan, and Sybase Central; a split screen provides a tree in the left panel and a detailed right panel. Testers were surprised to find that building DB2 clients without adding more components from IBM was quite easy. IBM supports the pure Java standard, and server-side Java support is provided. Testers determined that the core server design will definitely support SMP, **MPP** , and multi-terabyte, and learned from IBM that many large corporations are multi-terabyte users, although not under Windows NT.

PRICE: $399

COMPANY NAME: IBM Corp (351245)
SPECIAL FEATURE: Screen Layouts Tables Charts
DESCRIPTORS: Database Management; DB2; Parallel Processing; Program Development; Windows NT/2000
REVISION DATE: 20000830

21/5/4
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00106928 DOCUMENT TYPE: Review

PRODUCT NAMES: SpectraView 1000 (695203)

TITLE: SpectraView gets calibration right
AUTHOR: Fraser, Bruce
SOURCE: MacWEEK, v12 n8 p23(2) Feb 23, 1998
ISSN: 0892-8118
HOMEPAGE: http://www.macweek.com

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: A

SpectraView 1000 from Mitsubishi Electronics America is easy-to-use and offers accurate color calibration and comprehensive setup controls. SpectraView's calibration is at least as accurate as either the PressView 21SR from Radius Incorporated or the Barco Personal Calibrator Display according to measurements of a Minolta CA-100 Color Analyzer. SpectraView is capable of supporting resolutions of up to 1,600 by 1,200 dpi at a 75-Hz **vertical** scan frequency. This capability plus its calibration produces accurate, predictable color. One approach to calibrating monitors downloads a new look-up table to the video card. This approach causes the monitor to lose some addressable levels of brightness, particularly in the blue channel. The approach used by SpectraView overcomes this limitation. It uses a **serial connection** between the monitor and the host computer to gain direct control of the amplifiers on the monitor's voltage guns. Until now, only Radius and Barco used this kind of approach. Mitsubishi is the first major monitor manufacturer to use this approach with its SpectraView product. SpectraView lags behind its competitors in using beige instead of gray on its plastic bezel, and it offers no soft-proofing tools.

PRICE: $3995

COMPANY NAME: Mitsubishi Electronics America Inc (480134)
SPECIAL FEATURE: Photographs
DESCRIPTORS: Apple Macintosh; Color Matching; Graphics Tools; MacOS;

Screen Utilities
REVISION DATE: 20001130

21/5/5
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00105776 DOCUMENT TYPE: Review

PRODUCT NAMES: E-Term32 (691534)

TITLE: The Keys To True Emulation
AUTHOR: Hengey, Matt
SOURCE: HP Professional, v11 n10 p12(1) Oct 1997
ISSN: 0986-145X
HOMEPAGE: http://www.hppro.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Diversified Computer Systems' (DCSi's) E-Term32 is a 32-bit VT320, SCO ANSI terminal emulation and connectivity package for Windows 95 and Windows NT 4.0. E-Term32 provides a full-functioned FTP client with ping, traceroute, finger, whois, and NS Lookup utilities. The following connecetivity support is provided: direct serial up to 115,200 baud, TAPI modem support, TCP/IP using WinSock, and LAT using an optional poly/Net 32-bit LAT stack. E-Term32 operates over Microsoft's multithreaded TCP/IP stack for Windows 95 and Windows NT 4.0. A Session Manager allows creation and editing of named sessions, and as many as six emulation toolbar groups show on the screen in user-selected order. A DCL-type scripting language allows automation of login and file transfer tasks. The scripting language can be used with support for Dynamic Data Exchange client/server to support other application communications. Built-in support is provided for Kermit, XMODEM, YMODEM, and ZMODEM protocols. Therefore, file transfers can be done over **serial** or networked **connections** ; setup options control size, page positioning, and orientation of printed host reports. A system engineer who uses E-Term in a legal billing and accounting software company says his clients' ability to gain access to 132- **column** reports on 80- **column** screens without wraparound is a major advantage of E-Term32.

PRICE: $179

COMPANY NAME: Diversified Computer Systems Inc (DCSi) (349496)
SPECIAL FEATURE: Charts Screen Layouts
DESCRIPTORS: Data Communications; Enterprise Application Integration; File Transfer; IBM PC & Compatibles; Terminal Emulators; Windows; Windows NT/2000
REVISION DATE: 20010730

21/5/6
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00103167 DOCUMENT TYPE: Review

PRODUCT NAMES: Sybase SQL Server (695017); Sybase MPP **(659932); SQL Anywhere Professional (643025); Sybase IQ (631957); Enterprise Connect (512389**

TITLE: Sybase Warehousing
AUTHOR: Rennhackkamp, Martin
SOURCE: DBMS, v10 n9 p85(3) Aug 1997
ISSN: 1041-5173
HOMEPAGE: http://www.dbmsmag.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Sybase's Sybase SQL Server, Sybase **MPP** , SQL Anywhere Professional, Sybase IQ, and Enterprise Connect are among products highlighted in a discussion of warehousing tools from Sybase. Sybase's products include database servers optimized for the particular querying needs of interactive warehouses. They also include middleware for access to more than one data source. Integration and management of data movement and distribution within the enterprise warehouse environment is supported by InfoPump, a low-end data movement tool that summarizes and aggregates data before delivery to the warehouse. PowerBuilder, Power++, PowerJ, InfoMaker, and S-Designor (PowerDesigner) are also available. The tools support Sybase's interactive warehouse solutions which provide processes, products, and data from Sybase and other databases. The components are integrated into a comprehensive framework to gather data from many sources, including mainframe databases, applications, and external data sources. Sybase IQ (Interactive Query Accelerator) is the central data warehousing module. It is a DBMS server created specifically for decision support databases and advanced data analysis querying. It was built around Sybase's patented Bit-Wise query processing technology, and used sophisticated performance-optimized algorithms for advanced ad hoc queries. Data values are indexed in arrays of bits for each storage **column** , and are called Bit-Wise indexes.

COMPANY NAME: Sybase Inc (414981)
DESCRIPTORS: Data Warehouses; Database Management; Database Servers; Decision Support Systems; Information Retrieval; Middleware; PowerBuilder; Program Development; SQL Server
REVISION DATE: 20011130

21/5/7
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00100858 DOCUMENT TYPE: Review

PRODUCT NAMES: Teradata DBMS (414468); DB2 Parallel Edition (623253); DB2/6000 (441244); DB2 4 MVS (701866); Non-Stop SQL (311154); Sybase MPP **(659932**

TITLE: Taming Data Giants: Part 2
AUTHOR: Brobst, Stephen Robertson, Owen
SOURCE: DBMS, v10 n3 p63(6) Mar 1997
ISSN: 1041-5173
HOMEPAGE: http://www.dbmsmag.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

NCR's Teradata DBMS, IBM's DB2/6000 and DB2 Parallel Edition, and DB2 4 on MVS, Sybase's **MPP** , and Tandem Computers' Non-Stop SQL are products

highlighted in a discussion of techniques for management of mammoth databases. Three main methods are used to partition huge databases: hash, key-range, and round-robin partitioning. Hash requires a DBA to choose **columns** for each table to be used as input to a hashing function that determines the database partition upon which each table **row** will be assigned and stored. Key-range distributes data rows over the database partitions based on a preset key range related to each partition. Round robin is the easiest to implement of the three. It places rows in partitions as if the database were dealing out cards. Data is distributed efficaciously for high-volume loading or insert-selects into a large table. Straightforward activity means speed, so the round-robin method can distribute rows into a target table about 5 percent faster than the hashing method of partitioning. Teradata, DB2/6000 Parallel Edition, and **MPP** use the hash partitioning method for VLDB implementations. Other topics covered are Oracle 7.3's optimizer intelligence and syntactic extensions for improved efficiency; advantages and disadvantages of each partitioning method; 3-tier application design; Online Transaction Processing (OLTP) on shared-nothing databases; and intelligent indexing.

COMPANY NAME: NCR Corp (552798); IBM Corp (351245); Compaq Computer Corp (462977); Sybase Inc (414981)
DESCRIPTORS: Database Management; DB2; Distributed Processing; IBM; IBM RS/6000; MVS; Non-Stop Kernel; Parallel Processing; Program Development ; System Performance; Tandem; Teradata
REVISION DATE: 20020618

21/5/8
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00075891 DOCUMENT TYPE: Review

PRODUCT NAMES: MARC (558257); Abaqus (558265); MSC.Nastran (015830); MSC.Patran (010764)

TITLE: Analysis Tools in Tune with Design
AUTHOR: Beckert, Beverly A
SOURCE: Computer-Aided Engineering, v14 n3 p70(3) Mar 1995
ISSN: 0733-3536
HOMEPAGE: http://www.penton.com/cae/

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Analysis programs are used increasingly in design applications, as users have access to faster computer hardware, better software and graphics, and more intuitive interfaces. The developer of the Marc finite-element analysis (FEA) solvers agrees with other analysts that analysis products speed up simulation and offer several design alternatives. The vendor of the Abaqus FEA solvers agrees, and Ansys founder, John Swanson, states that more intuitive analysis software is also responsible. A spokesman for the developer of MSC/NASTRAN and MSC/Patran FEA/FEM products states that gradual hardware/software improvements mean that more engineers can use analysis products to shorten turnaround time and product cycles. Systems supporting scalable parallel processing (SPP) are available, providing massively parallel processing (**MPP**) system architecture in an easy to use environment. Future systems will be more automated and will support **vertical** applications.

COMPANY NAME: MSC.Software Corp (083780); Hibbitt Karlsson & Sorensen (603856)
DESCRIPTORS: CAD; CAD CAM; CAE; Engineering; FEA (Finite Element Analysis) ; Simulation
REVISION DATE: 20000823

21/5/9
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00070388 DOCUMENT TYPE: Review

PRODUCT NAMES: SNMP (830056)

TITLE: UPS Control Via SNMP Soon to Be Reality
AUTHOR: Stokinski, C Adam
SOURCE: Computer Technology Review, v14 n10 ps29(4) Oct 1994
ISSN: 0287-9647
HOMEPAGE: http://www.westworldproductions.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

UPS manufacturers have long provided SNMP with their proprietary MIBs. However, the IETF has now adopted a standard MIB, which will provide a more open means to achieve power management and control. The UPS-MIB can integrate any UPS into a centralized view of all power control points over a network. A UPS is a device that provides auxiliary power when **normal** utility power may be disrupted. Remote monitoring and manipulation of distributed control points from a central platform provides several needed conveniences for the network administrator. The older, one-on-one **serial connection** to the UPS would cause the system to execute its own shut-down routine. But connecting the UPS to the network means that the system must be shut down from the network itself. The UPS alarms are sent to the SNMP NMS management platform, instead of to the file server or host.

COMPANY NAME: Vendor Independent (999999)
SPECIAL FEATURE: Charts
DESCRIPTORS: Network Administration; Network Management; Network Software; Standards; System Monitoring
REVISION DATE: 20020630

21/5/10
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00070386 DOCUMENT TYPE: Review

PRODUCT NAMES: Operating Systems (830344)

TITLE: Growing Into Networking with Multiuser DOS
AUTHOR: Shalita, Steven P
SOURCE: Computer Technology Review, v14 n10 p16(3) Oct 1994
ISSN: 0287-9647
HOMEPAGE: http://www.westworldproductions.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis

GRADE: Product Analysis, No Rating

The LAN has become a common business tool. Client/server technology is also growing, as users require better methods of managing large amounts of data. This has resulted in a trend toward workgroup computing solutions being implemented within the LAN system. One popular method is use of an MDOS (multi-user DOS) systems. MDOS is used often in **vertical** markets and process control, and provides an alternative to LAN and UNIX technology. Many workgroups are using MDOS host systems with a centralized NetWare connection as a shared terminal workgroup. An MDOS system can be an effective platform for implementing database-intensive workgroups. They do not require the same transference of data from server to nodes as do LAN solutions. An MDOS system has only one PC with a single CPU for a host computer, and users have serial terminals on their desktop that are connected to the host by **serial connections** direct to the host.

COMPANY NAME: Vendor Independent (999999)
SPECIAL FEATURE: Charts
DESCRIPTORS: Client/server; LAN Alternatives; Network Software; Operating Systems
REVISION DATE: 19950228

21/5/11
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
(c)2002 Info.Sources Inc. All rts. reserv.

00064863 DOCUMENT TYPE: Review

PRODUCT NAMES: X Window (830048); Telecommuting (830232)

TITLE: Telecommuting by X
AUTHOR: Wood, Dave
SOURCE: X Journal, v3 n5 p36(6) May/Jun 1994
ISSN: 1056-7003

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

The X protocol can facilitate telecommuting, letting office workers bring office capabilities to their homes. The enabling technology for telecommuting is the ability to transfer the X protocol over a simple telephone line. In one computer company, telecommuting is widespread, with over 300 employees working from home at least part-time. Home-based workers employ the X Window system and X Remote, a proprietary protocol for remote **serial** X **connections** . The workers connect directly to the office network, as if they were physically in the office. The X Remote protocol has offered an improvement in speed and productivity. The X Remote process requires V.32 modems running at 9600 bps, and full-duplex modems are recommended to get the full advantage, since the X protocol is heavily **bidirectional** .

COMPANY NAME: Vendor Independent (999999)
DESCRIPTORS: Office Automation; Telecommunications; Telecommuting; X Window
REVISION DATE: 19990330

```
Set     Items   Description
S1      69113   MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCE-
             SSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGE-
             MENT? OR ORDER OR FORMATION)
S2       9780   (SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N-
             )(CONNECT? OR LINK?) OR SINGLE()BIT
S3      33901   MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUM-
             N?)
S4      80333   MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5       5948   MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DI-
             RECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6        191   VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7     995770   VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8    2521522   HORIZONTAL? OR ROW OR NORMAL?
S9     294552   BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR -
             PERPENDICULAR? OR STRAIGHT()LINE
S10         0   S1 AND S2 AND S3 AND S4 AND S5
S11        92   S1 AND S2
S12         0   S3 AND S4 AND S5 AND S6
S13         5   S3 AND S4 AND S5
S14         0   S11 AND S3
S15         0   S11 AND S4
S16         0   S11 AND S5
S17         0   S11 AND S6
S18     78801   S1 OR S2
S19         0   S18 AND S3 AND S4 AND S5
S20        80   S18 AND S3
S21        11   S20 AND S4
S22         0   S20 AND S5
S23         0   S20 AND S5
S24         0   S S18 AND S6
S25         0   S18 AND S6 AND S8 AND S9
S26         0   S18 AND S6
S27      2563   S18 AND S7
S28       611   S27 AND S8
S29         9   S28 AND S9
S30        28   S11 AND S7
S31         2   S30 AND S8
S32         3   S30 AND S9
S33        16   S13 OR S21
S34        35   S29 OR S30
S35        51   S33 OR S34
S36        47   S35 NOT PY>2000
S37        47   S36 NOT PD>20000831
S38        29   RD (unique items)
File 238:Abs. in New Tech & Eng. 1981-2002/Jul
         (c) 2002 Reed-Elsevier (UK) Ltd.
File   8:Ei Compendex(R) 1970-2002/Jul W4
         (c) 2002 Engineering Info. Inc.
File  77:Conference Papers Index 1973-2002/Jul
         (c) 2002 Cambridge Sci Abs
File  35:Dissertation Abs Online 1861-2002/Jun
         (c) 2002 ProQuest Info&Learning
File 202:Information Science Abs. 1966-2002/Jul 03
         (c) Information Today, Inc
File  65:Inside Conferences 1993-2002/Jul W4
         (c) 2002 BLDSC all rts. reserv.
File   2:INSPEC 1969-2002/Jul W4
         (c) 2002 Institution of Electrical Engineers
File  14:Mechanical Engineering Abs 1973-2002/Jul
         (c) 2002 Cambridge Sci Abs
```

File 94:JICST-EPlus 1985-2002/Jun W1
(c)2002 Japan Science and Tech Corp(JST)
File 6:NTIS 1964-2002/Aug W2
(c) 2002 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2002/Jul W4
(c) 2002 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 34:SciSearch(R) Cited Ref Sci 1990-2002/Jul W4
(c) 2002 Inst for Sci Info
File 62:SPIN(R) 1975-2002/Jul W1
(c) 2002 American Institute of Physics
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Jun
(c) 2002 The HW Wilson Co.
File 95:TEME-Technology & Management 1989-2002/Jul W4
(c) 2002 FIZ TECHNIK
File 239:Mathsci 1940-2002/Sep
(c) 2002 American Mathematical Society

38/5/1 (Item 1 from file: 238)
DIALOG(R)File 238:Abs. in New Tech & Eng.
(c) 2002 Reed-Elsevier (UK) Ltd. All rts. reserv.

0243332 ANTE NUMBER: 9303224
Parallel DFT computation on bit - serial **systolic** processor arrays
AUTHOR(S): Jones, K. J.
JOURNAL: IEE Proceedings E. Computers and Digital Techniques 140 (1) Jan 93 p.10-18. il.refs.
PUBLICATION YEAR: 1993
ISSN: 0143-7062
BLDSC SHELF MARK: 4362.7540
LANGUAGE: English

ABSTRACT: Shows how novel one- and two-dimensional systolic processing architectures can carry out hardware-efficient parallel implementation of the N-point discrete Fourier transform. Throughput rates are superior to the conventional linear array. The processor is in **bit - serial** form using **single - bit** half-adder and full-adder circuits, and comprises up to N coordinate rotation digital computer processing elements. (Original abstract-amended)

DESCRIPTORS: **Bit serial** systolic array processors; Solution; Discrete Fourier transforms;

38/5/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

05556384 E.I. No: EIP00055171379
Title: Extending a turbid medium BRDF model to allow sloping terrain with a vertical plant stand
Author: Combal, Bruno; Isaka, Harumi; Trotter, Craig
Corporate Source: Universite Blaise Pascal, Clermont-Ferrand, Fr
Source: IEEE Transactions on Geoscience and Remote Sensing v 38 n 2 I 2000. p 798-810
Publication Year: 2000
CODEN: IGRSD2 ISSN: 0196-2892
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 0007W1
Abstract: This paper extends the turbid medium approach used for **modeling bidirectional** reflectance from **horizontal** plant canopies to sloping terrain with a vertically oriented plant stand. Previous treatments have accounted for terrain slope by simple adaptation to an inclined plane of **models** for **horizontal** surfaces. However, such treatments implicitly assume that plants grow perpendicularly to the surface, despite the fact that plant stems continue to grow vertically on slopes. We investigate the differences between our new ' **vertical** growth' **model** and the more usual 'perpendicular to the surface growth' model in terms of the effect on canopy albedo and bidirectional reflectance factors. Although the effect of leaf angle distribution on the albedo is different for both the vertical-growth and **perpendicular** -growth **models** , it appears to be a much smaller effect than that due to terrain slope. For the bidirectional reflectance factors (BRF's), the magnitude and sign of the differences between the two models varies with the direction of observation, the slope, and the leaf angle distribution, and can exceed 10% for a planophile canopy. A comparison between modeled and measured data shows that **model** predictions under the **vertical** growth assumption are consistent with measurements, whereas the assumption of perpendicular growth can lead to

large errors. (Author abstract) 25 Refs.
Descriptors: *Plants (botany); Landforms; Optical properties; Mathematical models; Vegetation; Satellites; Image processing
Identifiers: Bidirectional reflectance factors; Albedo; Vertical plant stand; Sloping terrain
Classification Codes:
461.9 (Biology); 481.1 (Geology); 741.1 (Light/Optics); 921.6 (Numerical Methods); 655.2 (Satellites); 723.2 (Data Processing)
461 (Biotechnology); 481 (Geology & Geophysics); 741 (Optics & Optical Devices); 921 (Applied Mathematics); 655 (Spacecraft); 723 (Computer Software)
46 (BIOENGINEERING); 48 (ENGINEERING GEOLOGY); 74 (OPTICAL TECHNOLOGY); 92 (ENGINEERING MATHEMATICS); 65 (AEROSPACE ENGINEERING); 72 (COMPUTERS & DATA PROCESSING)

38/5/3 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

05472655 E.I. No: EIP00025009531
Title: Using emulations to enhance the performance of parallel architectures
Author: Obrenic, Bojana; Herbordt, Martin C.; Rosenberg, Arnold L.; Weems, Charles C.
Corporate Source: Queen's Coll, Flushing, NY, USA
Source: IEEE Transactions on Parallel and Distributed Systems v 10 n 10 1999. p 1067-1081
Publication Year: 1999
CODEN: ITDSEO ISSN: 1045-9219
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 0003W4
Abstract: We illustrate the potential of techniques and results from the theory of network emulations to enhance the performance of a parallel architecture. The vehicle for this demonstration is a suite of algorithms that endow an N-processor **bit - serial processor array** A with a `meta-instruction' GAUGE k, which (logically) reconfigures A into an N/k-processor virtual machine B//k that has: 1) a datapath and memory bus whose emulated width is k bits, as opposed to A's 1-bit width and 2) an instruction set that operates on k-bit words, in contrast to A's instruction set, which operates on 1-bit words. In order to stress the strength of the approach, we show (via pseudocode) how our emulation techniques can be implemented efficiently even if A operates in strict SIMD mode, with only **single - bit** masking capabilities and with no indexed memory accesses. We describe at an algorithmic level how to implement our technique - including datapath conversion (`corner-turning') and the creation of the word-parallel instruction sets - on arrays of any regular network topology. We instantiate our technique in detail for arrays based on topologies with quite disparate characteristics: the hypercube, the de Bruijn network, and a genre of mesh with reconfigurable buses. Importantly, the emulations that underlie our technique do not alter the native machine's instruction set, hence allowing an invariant programming model across gauges. (Author abstract) 30 Refs.
Descriptors: *Parallel processing systems; Computer architecture; Parallel algorithms; Electric network topology; Interconnection networks; Computer systems programming
Identifiers: Parallel architectures; Multiprocessor interconnection
Classification Codes:
722.4 (Digital Computers & Systems); 703.1 (Electric Networks); 723.1 (Computer Programming)

722 (Computer Hardware); 723 (Computer Software); 921 (Applied Mathematics); 703 (Electric Circuits)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 70 (ELECTRICAL ENGINEERING)

38/5/4 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

03310421 E.I. Monthly No: EI9110118900
Title: Efficient compensation-path finding algorithm for a large-scale processor array .
Author: Ozawa, Takao
Corporate Source: Kyoto Univ, Kyoto, Jpn
Source: Systems and Computers in Japan v 22 n 1 1991 p 28-38
Publication Year: 1991
CODEN: SCJAEP ISSN: 0882-1666
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications); X; (Experimental)
Journal Announcement: 9110
Abstract: This paper presents an algorithm for constructing a systolic array from a large-scale rectangular grid array of processing elements (PEs), some of which may be faulty. Very recently, Kung et al. reduced this construction problem to finding compensation paths (CPs) which are extended from faulty PEs to spare PEs placed on the periphery of the rectangular array, and which satisfy the following conditions. Each of the CPs: (1) must be a **horizontal** or **vertical straight line** ; (2) must not go through any other faulty **PE** ; (3) must not cross any other CP; and (4) for each of the CPs there exists no other CP running in parallel and in the **opposite direction** with distance 1. The algorithm of this paper solves the foregoing CP finding problem efficiently by taking advantage of certain properties of the grid array. Suppose that the array is placed on the x-y plane. First, the algorithm sorts the faulty PEs with respect to their x and y coordinates and constructs four queues for faulty PEs. Then it attempts repeatedly to find CPs for the four PEs at the exists of the four queues. At this step it uses a novel branch-and-bound method considering the relative positions of the four faulty PEs on the x-y plane. The time complexity of the algorithm is O(n**3) in the worst cases, where n is the number of faulty PEs. However, it can be shown that such cases rarely happen, and in almost all cases it solves the problem in O(n**2) time. The space complexity is O(n). (Author abstract)
Descriptors: *DATA STORAGE, DIGITAL--*Cellular Arrays; MATHEMATICAL TECHNIQUES--Algorithms; COMPUTERS--Circuits
Identifiers: PROCESSING ELEMENTS (**PE**); COMPENSATION PATH (CP); SYSTOLIC ARRAYS
Classification Codes:
721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics); 722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

38/5/5 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

03073049 E.I. Monthly No: EI9106069396
Title: Representing and computing regular languages on massively parallel networks.
Author: Miller, Michael I.; Roysam, Badrinath; Smith, Kurt R.;

O'Sullivan, Joseph A.
Corporate Source: Dept of Electr Eng, Washington Univ, St Louis, MO, USA
Source: IEEE Transactions on Neural Networks v 2 n 1 Jan 1991 p 56-72
Publication Year: 1991
CODEN: ITNNEP ISSN: 1045-9227
Language: English
Document Type: JA; (Journal Article) Treatment: L; (Literature Review/Bibliography); T; (Theoretical)
Journal Announcement: 9106
Abstract: A general method is proposed for incorporating rule-based constraints corresponding to regular languages into stochastic inference problems, thereby allowing for a unified representation of stochastic and syntactic pattern constraints. The authors' approach establishes the formal connection of rules to Chomsky grammars and generalizes the original work of Shannon on the encoding of rule-based channel sequences to Markov chains of maximum entropy. This maximum entropy probabilistic view leads to Gibbs representations with potentials which have their number of minima growing at precisely the exponential rate that the language of deterministically constrained sequences grow. These representations are coupled to stochastic diffusion algorithms, which sample the language-constrained sequences by visiting the energy minima according to the underlying Gibbs probability law. The coupling to stochastic search methods yields the all-important practical result that fully parallel stochastic cellular automata can be derived to generate samples from the rule-based constraint sets. The production rules and neighborhood state structure of the language of sequences directly determine the necessary connection structures of the required parallel computing surface. Representations of this type have been mapped to the DAP-510 **massively parallel processor** consisting of 1024 mesh- **connected bit - serial** processing elements for performing automated segmentation of electron-micrograph images. 66 Refs.
Descriptors: *NEURAL NETWORKS; AUTOMATA THEORY--Formal Languages; PROBABILITY--Random Processes; IMAGE PROCESSING; COMPUTER PROGRAMMING--Algorithms
Identifiers: MASSIVELY PARALLEL NETWORKS; RULE BASED CONSTRAINTS; STOCHASTIC INFERENCE PROBLEMS
Classification Codes:
723 (Computer Software); 721 (Computer Circuits & Logic Elements); 922 (Statistical Methods)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

38/5/6 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

02954861 E.I. Monthly No: EI9009105747
Title: Bit - serial **VLSI array processing chip for image processing.**
Author: Heaton, Robert; Blevins, Donald; Davis, Edward
Corporate Source: Microelectronics Cent of North Carolina, Research Triangle Park, NC, USA
Source: IEEE Journal of Solid-State Circuits v 25 n 2 Apr 1990 p 364-368
Publication Year: 1990
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9009
Abstract: An array processing chip integrating 128 **bit - serial** processing elements (PEs) on a single die is discussed. Each **PE** has a 16-function logic unit, a **single - bit** adder, a 32-b variable-length shift register, and 1 kb of local RAM. Logic in each **PE** provides the

capability to mask PEs individually. A modified grid interconnection scheme allows each **PE** to communicate with each of its eight nearest neighbors. A 32-b bus is used to transfer data to and from the array in a single cycle. Instruction execution is pipelined, enabling all instructions to be executed in a single cycle. The 1- mu m CMOS design contains over 1.1-million transistors on an 11.0-mm multiplied by 11.7-mm die. 4 Refs.

Descriptors: *INTEGRATED CIRCUITS, VLSI--*Performance; IMAGE PROCESSING; LOGIC CIRCUITS; DATA STORAGE, DIGITAL--Random Access; SEMICONDUCTOR DEVICES, MOS

Identifiers: SINGLE DIE; **SINGLE - BIT** ADDER; SINGLE CYCLE; 1.1-MILLION TRANSISTORS; VLSI ARRAY; RAM

Classification Codes:

713 (Electronic Circuits); 714 (Electronic Components); 723 (Computer Software); 741 (Optics & Optical Devices); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)

38/5/7 (Item 6 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

(c) 2002 Engineering Info. Inc. All rts. reserv.

02837523 E.I. Monthly No: EIM8912-048770

Title: BLITZEN: a VLSI array processing chip.

Author: Heaton, Robert A.; Blevins, Donald W.

Corporate Source: Microelectron Cent, Research Triangle Park, NC, USA

Conference Title: Proceedings of the IEEE 1989 Custom Integrated Circuits Conference

Conference Location: San Diego, CA, SA Conference Date: 19890515

Sponsor: IEEE, Electron Devices Soc, New York, NY, USA; IEEE, Solid-State Circuits Council, USA; IEEE, Rochester Section, USA

E.I. Conference No.: 12624

Source: Proceedings of the Custom Integrated Circuits Conference. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2671-6), Piscataway, NJ, USA. p 12.1/1-5

Publication Year: 1989

CODEN: PCICER ISSN: 0886-5930

Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 8912

Abstract: An array processing chip for the BLITZEN massively parallel SIMD (single-instruction multiple-data-stream) computer has been developed. The chip includes 128 **bit - serial** processing elements (PEs) connected in a modified grid. Each **PE** contains a 16-function logic unit, a **single - bit** adder, a 32-bit, variable-length shift register, and 1k of local RAM. The 1- mu m CMOS design contains over 1.1 million transistors on a 110-mm by 11.7-mm die. 5 Refs.

Descriptors: *INTEGRATED CIRCUITS, VLSI--*Performance; COMPUTERS, DIGITAL

Identifiers: ARRAY PROCESSING CHIP; SIMD (SINGLE-INSTRUCTION MULTIPLE-DATA-STREAM)

Classification Codes:

713 (Electronic Circuits); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

38/5/8 (Item 7 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

(c) 2002 Engineering Info. Inc. All rts. reserv.

02185287 E.I. Monthly No: EI8704031982
Title: MOBILE-PHASE OPTIMIZATION IN GRADIENT-ELUTION HPLC FOR THE SEPARATION OF THE PHENYLTHIOHYDANTOIN-AMINO ACIDS.
Author: Glajch, J. L.; Kirkland, J. J.
Corporate Source: DuPont, Wilmington, DE, USA
Source: Journal of Chromatographic Science v 25 n 1 Jan 1987 p 4-11
Publication Year: 1987
CODEN: JCHSBZ ISSN: 0021-9665
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: X; (Experimental)
Journal Announcement: 8704
Abstract: A general method for optimizing gradient-elution separations is described and applied to the specific separation of the 20 PTH-amino acid derivatives. The optimum separation of these compounds is shown to be performed in 25 min using a **PE column** with a ternary gradient containing phosphate buffer, methanol, and tetrahydrofuran as the mobile phase. The specific optimized gradient-elution separation is compared to a previously reported optimized isocratic separation, and advantages of each system are compared. Additional influences on separation selectivity for the PTH-amino acids, such as ionic strength and the use of **serially connected columns** , are also investigated. (Author abstract) 24 refs.
Descriptors: *AMINO ACIDS--*Chromatographic Analysis; SEPARATION--Optimization; CHROMATOGRAPHIC ANALYSIS--Liquid
Identifiers: MOBILE-PHASE OPTIMIZATION; PHENYLTHIOHYDANTOIN-AMINO ACIDS; STATIONARY PHASE SELECTIVITY
Classification Codes:
804 (Chemical Products); 801 (Chemical Analysis & Physical Chemistry); 802 (Chemical Apparatus & Plants)
80 (CHEMICAL ENGINEERING)

38/5/9 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2002 Engineering Info. Inc. All rts. reserv.

01348370 E.I. Monthly No: EI8305035884 E.I. Yearly No: EI83059662
Title: INFLUENCE OF PLANETARY BOUNDARY LAYER PHYSICS ON FRONTAL STRUCTURE IN THE HOSKINS-BRETHERTON HORIZONTAL **SHEAR** MODEL .
Author: Keyser, Daniel; Anthes, Richard A.
Corporate Source: Pa State Univ, University Park, USA
Source: Journal of the Atmospheric Sciences v 39 n 8 Aug 1982 p 1783-1802
Publication Year: 1982
CODEN: JAHSAK ISSN: 0099-7005
Language: ENGLISH
Journal Announcement: 8305
Abstract: A series of numerical experiments with the Hoskins-Bretherton **horizontal** shear **model** of frontogenesis in an amplifying, two-dimensional baroclinic wave is performed. The analytic solutions from the Boussinesq, semi-geostrophic model provide initial conditions for numerical integrations with a two-dimensional, dry version of the fully compressible, hydrostatic primitive equation (**PE**) model of Anthes and Warner with 40 km **horizontal** resolution. The **PE model** is integrated 1) without planetary boundary layer (PBL) physics; 2) with a one-layer bulk-drag scheme; and 3) with a high- **vertical** -resolution PBL **model** . The lower boundary is thermally insulated in order to isolate the effect of the internal mixing of heat in the PBL. The simulation with the high-resolution PBL physics resolves several realistic features. 37 refs.
Descriptors: *METEOROLOGY
Classification Codes:
443 (Meteorology)

44 (WATER & WATERWORKS ENGINEERING)

38/5/10 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2002 ProQuest Info&Learning. All rts. reserv.

01391849 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
INTERNAL SEICHES AND BAROCLINIC CURRENTS IN LAKE BANYOLES (SPAIN)
Original Title: SEQUES INTERNES I CORRENTS BAROCLINICS A L'ESTANY DE BANYOLES

Author: ROGET I ARMENGOL, ELENA
Year: 1992
Corporate Source/Institution: UNIVERSITAT AUTONOMA DE BARCELONA (SPAIN) (5852)
Source: VOLUME 56/01-C OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 86. 303 PAGES
Descriptors: BIOLOGY, LIMNOLOGY
Descriptor Codes: 0793
Language: SPANISH
ISBN: 84-7929-533-3
Publisher: SERVEI DE PUBLICACIONS DE LA UNIVERSITAT AUTONOMA DE BARCELONA, EDIFICI RECTORAT, APARTAT POSTAL 20, E-08193 BELLATERRA (BARCELONA), SPAIN

This is the first time that the internal seiches in Lake Banyoles (A = 112 $\rm Hm\sp2,$ V = 16 $\rm Hm\sp3)$ have been described. For their study a unidimensional model of two layers and two bidimensional models of two and three layers have been used. During the summer, the metalimnion is very thick and the lake reacts as composed by three layers and the second **vertical mode** is excited. In this case, the maximum amplitude of the vertical displacements at the lower interface of the metalimnion--between 1 and 2 m--is always higher--up to 5 times--the vertical displacements at the upper interface. In Lake Banyoles the second **vertical mode** propagates either in the direction of the main axis of the lake (longitudinal **mode**) or **perpendicular** to that (transversal **mode**) depending on the wind which forces the set-up. From the end of August to half of October, the period of this second **vertical mode** when it develops as the first **horizontal** longitudinal **mode** is of between 4 and 7 hours, while that of the second **horizontal** longitudinal **mode** is of between 2 and 4 hours, approximately. The period of the first transversal mode is always very close to the second longitudinal but a little smaller. The observed amplitudes are of about 1 metre.

Because of the different relation between the area and the volume in the northern and the southern lobes, and because of the difference in the heat inflow coming from the underground sources at the two lobes, the northern lobe cools quicker than the southern. This fact forces a baroclinic or density current which flows from north to south.

Either from direct current--at the neck between the two lobes velocities up to 12 cm/s and with daily mean values of about 5 cm/s are measured--and temperature measurements or from a heat balance where the whole lake is considered to be composed by two homogeneous systems (the northern and the southern lobes) which are connected between them, a baroclinic current of the order of $10\sp4$ l/s is found and thus, the water in the northern lobe is renovated about every five days. Thus, it is expected that this baroclinic current, because of its magnitude, apart of reducing the differences between the two lobes, influences the lakewide circulation. (Abstract shortened by UMI.)

38/5/11 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2002 ProQuest Info&Learning. All rts. reserv.

757377 ORDER NO: AAD81-20445

FRONTOGENESIS IN THE PLANETARY BOUNDARY LAYER OF AN AMPLIFYING, TWO-DIMENSIONAL BAROCLINIC WAVE

Author: KEYSER, DANIEL
Degree: PH.D.
Year: 1981
Corporate Source/Institution: THE PENNSYLVANIA STATE UNIVERSITY (0176)
Source: VOLUME 42/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1497. 314 PAGES
Descriptors: PHYSICS, ATMOSPHERIC SCIENCE
Descriptor Codes: 0608

Despite recent theoretical advances in understanding the dynamics of surface frontogenesis, considerable discrepancies remain between the idealized frontal structures derived from the two-dimensional, isentropic, inviscid frontogenesis models and the detailed structures revealed through observational studies. In order to explore the hypothesis that the absence of fine structure is related to the neglect of nonconservative processes such as the vertical turbulent transports of heat and momentum in the planetary boundary layer (PBL), a series of analytic and numerical experiments with the Hoskins-Bretherton **horizontal** shear **model** of frontogenesis in an amplifying, two-dimensional baroclinic wave is performed.

The analytic solutions from the Boussinesq, semi-geostrophic Hoskins-Bretherton **horizontal** shear **model** under the restriction of uniform buoyancy frequency are reproduced in order to provide initial conditions for, and a control case for comparison with, numerical integrations obtained with a two-dimensional, dry version of the fully compressible, hydrostatic primitive equation (**PE**) model of Anthes and Warner integrated with 40-km **horizontal** resolution. The **PE model** is integrated (1) without PBL physics; (2) with a one-layer bulk-drag scheme; and (3) with a high- **vertical** -resolution PBL **model** . In both alternatives utilizing PBL physics, the lower boundary is thermally insulated in order to isolate the effect of the internal mixing of heat in the PBL.

Surface frontogenesis in the analytic **horizontal** shear **model** is diagnosed quantitatively in terms of the prognostic equations for the relative vorticity, the cross-front gradient of potential temperature, and the stability. Frontogenesis is interpreted as a geostrophic adjustment process in which the components of the thermal wind relation, representing the mass and wind fields, continuously adjust to imbalances forced by the frontogenetical geostrophic horizontal shear through a thermally direct ageostrophic circulation in the cross-front, vertical plane. The energetics of the finite-amplitude baroclinic wave containing the frontal zone are examined in order to search for an explanation for the subordinate role of frontolytical vertical motions compared to the frontogenetical horizontal component of the ageostrophic circulation. The wavenumber-dependent disturbance growth rate is expressed in terms of upward and northward fluxes of heat and momentum, and an explanation for the shortwave cutoff in the model is proposed.

The simulation with the high-resolution PBL physics is able to resolve several realistic features including (1) a narrow updraft at the top of the PBL above the sea-level pressure trough at the warm edge of the frontal zone; (2) a stable layer capping the PBL to the rear of the frontal zone; and (3) slightly unstable or neutral lapse rates in the PBL behind the front and stable lapse rates in the PBL ahead of the front. A diagnostic analysis of the frontogenesis indicates that the fine structure resulting from adding PBL physics can be attributed to the frictionally

driven, ageostrophic inflow in the PBL toward the surface pressure trough in which the frontal zone is located. A finding of particular interest is that the stability patterns in the PBL on either side of the front evolve independently of sensible heating through the lower boundary.

The results of this investigation suggest two hypotheses: The first relates the orientation of cloud bands associated with low-level frontal zones to the frontogenetical mechanisms of horizontal shear and confluence. The second is concerned with explaining the structure and evolution of several atmospheric circulation systems in terms of adjustment processes toward equilibrium configurations between the mass and wind fields.

38/5/12 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

4904863 INSPEC Abstract Number: C9504-4230M-053
Title: Simulation of a tree structure interconnection network
Author(s): Vakilzadian, H.; Sharif, H.
Author Affiliation: Dept. of Electr. Eng., Nebraska Univ., Lincoln, NE, USA
p.960-4
Editor(s): Pace, D.K.; Fayek, A.-M.
Publisher: SCS, San Diego, CA, USA
Publication Date: 1994 Country of Publication: USA xix+972 pp.
Conference Title: Proceedings of 1994 Summer Computer Simulation Conference
Conference Sponsor: SCS
Conference Date: 18-20 July 1994 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: A simulation study of a tree-structured interconnection network suitable for connecting an array of processors and memory modules (nodes) is presented. The links interconnecting the nodes are high-speed bi-directional **serial links** . A network of switches is used to connect the links to the processors and memory modules. The inner **column** of switches are connected point-to-point (in a mesh), whereas the outer **columns** are connected in a binary tree topology. This paper describes a simulation study of the performance of this network. The results have been compared against a mesh-type (fully interconnected) network for cost-effectiveness and link utilization. (6 Refs)
Subfile: C
Descriptors: multiprocessor interconnection networks; performance evaluation; switched networks; trees (mathematics); virtual machines
Identifiers: tree-structured interconnection network; simulation; **processor array** ; memory module array; high-speed bidirectional **serial links** ; switch network; point-to-point connection; binary tree topology; network performance; mesh-type network; fully interconnected network; cost-effectiveness; link utilization
Class Codes: C4230M (Multiprocessor interconnection); C7430 (Computer engineering); C5670 (Network performance); C5470 (Performance evaluation and testing)
Copyright 1995, IEE

38/5/13 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

00822397 INSPEC Abstract Number: C75025988
Title: Mixed mode arithmetic for STARAN
Author(s): Stabler, E.P.
Author Affiliation: Dept. of Electrical & Computer Engng., Syracuse Univ., Syracuse, NY, USA
Conference Title: Parallel Processing p.228-9
Editor(s): Feng, T.
Publisher: Springer-Verlag, Berlin, West Germany
Publication Date: 1975 Country of Publication: West Germany vi+433 pp.
ISBN: 3 540 07135 0
Conference Date: 20-23 Aug. 1974 Conference Location: Raquette Lake, NY, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P); Theoretical (T)
Abstract: The array memory of STARAN can provide data to the arithmetic processing equipment in **bit serial mode** , word **mode** or mixed mode. In the mixed mode system analysed here the memory provides 32 words of 32 bits for parallel processing. It is different from the **normal** bit **mode** operation for STARAN in which the system processes a **single bit** of each of the 1024 data words at a given moment. The STARAN system analysed here has an array memory size of 1024*1024 bits, which is segmented into 4 subarrays of 256*1024. (0 Refs)
Subfile: C
Descriptors: digital arithmetic; parallel processing
Identifiers: arithmetic processing; **bit serial mode** ; word mode; mixed mode; parallel processing; STARAN processor; mixed mode arithmetic
Class Codes: C5230 (Digital arithmetic methods); C5400 (Analogue and digital computers and systems)

38/5/14 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

04485697 JICST ACCESSION NUMBER: 00A0170902 FILE SEGMENT: JICST-E
Phase Characterization and Thermal Conductivity of Carbon Alloys Obtained by Interface Reaction between C/C Composites and Pressed Molybdenum Silicide.
YAMAMOTO OSAMU (1); SUGANO KAZUYUKI (1); SASAMOTO TADASHI (1); OTA NAOTO (2); SOGABE TOSHIAKI (2)
(1) Kanagawa Inst. of Technology; (2) Toyo Tanso Co., Ltd.
Tanso, 1999, NO.190, PAGE.246-251, FIG.5, TBL.2, REF.14
JOURNAL NUMBER: G0633AAG ISSN NO: 0371-5345 CODEN: TASOA
UNIVERSAL DECIMAL CLASSIFICATION: 661.66
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The C/C composites made by laying up the sheets of carbon fibers using a pitch matrix were used as starting materials. After cutting the composites in the parallel (PA) and the **perpendicular** (**PE**) directions to the sheets of carbon fibers, the surface of PA and **PE** substrates obtained were reacted with MoSi2 at 1450.DEG.C. in argon gas. From XRD measurements, the four phases of graphite, MoSi2, MoO3 and .ALPHA.-SiC were observed at the surface of the substrates treating for 3 and 6h, irrespective of the direction to carbon fiber sheets. A concentration gradient of SiC in the as-prepared substrates was observed in both directions parallel and **perpendicular** ; the concentration of SiC decreases along the depth from the surface of

substrate. In the results of line analysis by EDX measurements, it was found that the reaction between C/C substrates and MoSi2 occurred in the portion of matrix in the substrates. The thermal conductivity of PA substrates decreased with the increase of the treating time and was lower than that of PA substrate without treatment. However, the thermal conductivity of the **PE** substrates treating for 6h was higher than that of the PA substrates treating below 3h and without treatment. (author abst.)
DESCRIPTORS: carbon-carbon composites; molybdenum silicide; thermal conductivity; thermochemical reaction; micro structure; carbon fiber; fabric; **vertical** direction; **horizontal** ; surface reaction; interface(surface); nuclear fusion reactor wall; temperature dependence ; silicon carbide
BROADER DESCRIPTORS: composite material; material; silicide; silicon compound; carbon group element compound; molybdenum compound; 6A group element compound; transition metal compound; heat transmission coefficient; coefficient; ratio; transport coefficient; chemical reaction; structure; carbon material; inorganic material; inorganic man made fiber; man-made fiber; fiber; high temperature fiber; textile product; product; direction; heterogeneous reaction; face; furnace wall ; wall; furnace component; dependence; carbide; carbon compound
CLASSIFICATION CODE(S): YB02060D

38/5/15 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2002 Japan Science and Tech Corp(JST). All rts. reserv.

03622370 JICST ACCESSION NUMBER: 98A0653584 FILE SEGMENT: JICST-E
A Linear Synchronous Motor and Position Sensorless Control for Horizontal **and** Vertical **Consecutive Transport.**
OSAWA HIROSHI (1); WATANABE TOSHIHARU (1)
(1) Fuji Electr. Corp. Res. & Dev. Ltd.
Denki Gakkai Kinzoku Sangyo Kenkyukai Shiryo, 1998, VOL.MID-98,NO.11-16, PAGE.13-19, FIG.12, TBL.2, REF.7
JOURNAL NUMBER: X0770AAD
UNIVERSAL DECIMAL CLASSIFICATION: 621.867 621.313.13 62-531
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: As the verification model of the big depth transport system by linear synchronous motor(LSM), the authors developed the experimental equipment of 3000N driving force. The LSM drive system consists of ten armatures and two inverters. The carriage can move between the **horizontal** track and the **vertical** track **consecutively** , by **connecting** both tracks with the curvilinear armature. At this equipment, position sensors are installed only on the **straight line** parts, and position sensor less control is performed on the curvilinear parts. Good characteristics have been confirmed by the eigenvalue analysis and the experiment. (author abst.)
DESCRIPTORS: linear motor; synchronous motor; elevating conveyor; trolley conveyor; position control; speed control; inverter fed motor drive; position sensor; running performance; armature
BROADER DESCRIPTORS: motor; electric machine; machinery; electric power equipment; AC motor; AC machine; synchronous machine; conveyor; transporting machine; chain conveyor; control; drive; operation and driving; electric power equipment operation; operation(processing); sensor; instrumentation element; performance
CLASSIFICATION CODE(S): QE01030Q; NB07030U; IC03030Q

38/5/16 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
(c) 2002 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1797412 NTIS Accession Number: N94-22901/0
Conception d'Architectures Integrees de Traitement d'Image de Bas Niveau (Design of Integrated Architectures for Low Level Image Processing)
(Ph.D. Thesis)
Boubekeur, A.
Institut National Polytechnique de Grenoble (France).
Corp. Source Codes: 039436000; II427835
Report No.: ETN-94-95183
1992 177p
Languages: French Document Type: Thesis
Journal Announcement: GRAI9412; STAR3206
Text in French.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A09/MF A02
Country of Publication: France
Methods and tools for the design of massively parallel low level image processing integrated systems are presented. The design of a programmable two dimensional array of 6720 **single bit** Processors (**PE** 's) implemented on a wafer is addressed. Two level defect tolerance techniques were used. At a subsystem level, a spare **column** is provided to replace defective **PE** 's. At the wafer level, an original switching network (externally controlled) is used to bypass defective subarrays. A high level synthesis tool is used to synthesize automatically from a behavioral specifications a dedicated array from a specific application. Resources in terms of registers, connections (multiplexers), and memory points are minimized.
Descriptors: *Architecture (Computers); *Image processing; *Integrated circuits; Central processing units; Fault tolerance; Simd (Computers); Switching theory; Wafers
Identifiers: *Foreign technology; Theses; NTISNASAE
Section Headings: 62F (Computers, Control, and Information Theory--Pattern Recognition and Image Processing); 62A (Computers, Control, and Information Theory--Computer Hardware)

38/5/17 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
(c) 2002 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1333155 NTIS Accession Number: N87-29135/7
Supercomputing on Massively Parallel Bit - Serial **Architectures**
Iobst, K.
National Aeronautics and Space Administration, Washington, DC.
Corp. Source Codes: 011249000; NC452981
Aug 85 22p
Languages: English
Journal Announcement: GRAI8801; STAR2523
In Its Proceedings: Computer Science and Data Systems Technical Symposium, v1 22p.
NTIS Prices: (Order as N87-29124/1, PC A16/MF A01)
Country of Publication: United States
Research on the Goodyear **Massively Parallel Processor** (**MPP**) suggests that high-level parallel languages are practical and can be

designed with powerful new semantics that allow algorithms to be efficiently mapped to the real machines. For the **MPP** these semantics include parallel/associative array selection for both dense and sparse matrices, variable precision arithmetic to trade accuracy for speed, micro-pipelined train broadcast, and conditional branching at the processing element (**PE**) control unit level. The preliminary design of a FORTRAN-like parallel language for the **MPP** has been completed and is being used to write programs to perform sparse matrix array selection, min/max search, matrix multiplication, Gaussian elimination on **single bit** arrays and other generic algorithms. A description is given of the **MPP** design. Features of the system and its operation are illustrated in the form of charts and diagrams.

Descriptors: *Architecture (Computers); *High level languages; *Parallel computers; Algorithms; Design analysis; Matrices (Mathematics); Semantics

Identifiers: Supercomputers; NTISNASA

Section Headings: 62B (Computers, Control, and Information Theory--Computer Software); 62A (Computers, Control, and Information Theory--Computer Hardware)

38/5/18 (Item 3 from file: 6)

DIALOG(R)File 6:NTIS

(c) 2002 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1306330 NTIS Accession Number: AD-A180 509/2

Numerical Studies of Frontal Dynamics

(Final rept. 1 Nov 83-30 Nov 86)

Keyser, D.

National Aeronautics and Space Administration, Greenbelt, MD. Goddard Space Flight Center.

Corp. Source Codes: 013129001; 156200

Sponsor: Air Force Office of Scientific Research, Bolling AFB, DC.

Report No.: AFOSR-TR-87-0685

31 Dec 86 13p

Languages: English

Journal Announcement: GRAI8717

Sponsored in part by Grants AFOSR-ISSA-85-0008 and AFOSR-ISSA-86-0019.

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A02/MF A01

Country of Publication: United States

Contract No.: AFOSR-ISSA-84-0012; AFOSR-ISSA-85-0077; 2310; A1

Efforts concentrated on the development of a two dimensional primitive equation (**PE**) model of frontogenesis that simultaneously incorporates the frontagenetical mechanisms of confluence and **horizontal** shear. Applying this **model** to study the effects of upper level frontogenesis, it appeared to be dominated by tilting effects associated with cross front variation of vertical motion, in which subsidence is maximized within and to the warm side of the frontal zone. Results suggest that aspects characteristics of three-dimensional barolinic waves may be abstracted to a significant extent in a two dimensional framework. They also show that upper-level frontogenesis and tropopause folding can occur in the absence of three-dimensional curvature effects, commonly believed to be necessary for realistic upper-level frontogenesis. An implication of the dominant tilting effects is that they may have to be adequately resolved by numerical weather prediction **models** , thus requiring better **horizontal** and vertical resolution. Keywords: Frontogenesis; Primitive equation model; Tilting; Confluence; Shear.

Descriptors: Fronts(Meteorology); Equations; Horizontal orientation;

Shear properties; Numerical analysis; Curvature; Three dimensional; Folding ; Tropopause; Mathematical models; Confluence; Weather forecasting; Tilt; Motion; **Vertical** orientation; Atmosphere **models**

Identifiers: Frontogenesis; Primitive equation models; NTISDODXA; NTISDODAF

Section Headings: 55C (Atmospheric Sciences--Meteorological Data Collection, Analysis, and Weather Forecasting); 55B (Atmospheric Sciences--Dynamic Meteorology)

38/5/19 (Item 4 from file: 6)

DIALOG(R)File 6:NTIS

(c) 2002 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1293106 NTIS Accession Number: DE87002403

Renovation of Dilute Process Wastewaters: Mini-Pilot Plant Evaluation of an Integrated Process System to Meet the Clean Water Act's Heavy-Metal and Organic Treatment Requirements at Oak Ridge National Laboratory

Begovich, J. M. ; Brown, C. H. ; Villiers-Fisher, J. F. ; Thompson, W. T. ; Patrick, G. C.

Oak Ridge National Lab., TN.

Corp. Source Codes: 021310000; 4832000

Sponsor: Martin Marietta Energy Systems, Inc., Oak Ridge, TN.; Engineering-Science, Inc., Atlanta, GA.; Department of Energy, Washington, DC.

Report No.: CONF-861066-1

1986 13p

Languages: English Document Type: Conference proceeding

Journal Announcement: GRAI8712; NSA1200

47. international water conference, Pittsburgh, PA, USA, 27 Oct 1986.

Portions of this document are illegible in microfiche products. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A02/MF A01

Country of Publication: United States

Contract No.: AC05-84OR21400

The purpose of the facility was to simulate the treatment the ORNL nonradiological wastewaters will receive in the NRWT plant. In the **MPP** , all wastewaters, with the exception of those not containing heavy metals (i.e., Cd, Cr, Cu, Fe, Pb, Hg, Ni, Ag, and Zn), flowed through an API-type separator. The criteria metals (except for mercury) were removed in the reactor/clarifier (R/C) as hydroxide precipitates using either calcium hydroxide (lime) and sodium carbonate (soda ash) or sodium hydroxide (caustic). Overflow from the precipitator was then treated by dual-media (sand and anthracite) filters and adjusted to a pH of 7. Wastewaters that had been pretreated by ion exchange for radionuclide removal bypassed the first four unit operations and were combined with the other wastewaters prior to air stripping. Volatile organics were removed by air stripping in a packed tower, while heavy (nonvolatile) organics and mercury were removed in three **serially connected** GAC **columns** . An ion-exchange (IX) **column** was operated in parallel with the R/C in order to evaluate the long-term performance of a chelating, heavy-metal-selective resin. In general, results of the **MPP** studies correlated well with those of the bench-scale treatability studies. The remainder of this paper details: the results of selected bench-scale treatability studies; spiking of feed streams; the **MPP** flowsheet and description of equipment; the results from the two **MPP** campaigns; and finally, the conclusions formulated by this treatability work. (ERA citation 12:012343)

Descriptors: *ORNL; *Waste Water; Chemical Effluents; Clean Water Act;

Compliance; Liquid Wastes; Organic Compounds; Waste Management
Identifiers: *Water pollution control; *Heavy metals; *Waste treatment; ERDA/520600; ERDA/520500; NTISDE
Section Headings: 68D (Environmental Pollution and Control--Water Pollution and Control)

38/5/20 (Item 5 from file: 6)
DIALOG(R)File 6:NTIS
(c) 2002 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1045514 NTIS Accession Number: N83-25378/1
Massively Parallel Processor **Computer**
(Patent)
Fung, L. W.
National Aeronautics and Space Administration, Greenbelt, MD. Goddard Space Flight Center.
Corp. Source Codes: 013129001; NC999967
Report No.: PATENT-4 380 046; PAT-APPL-6-041 143,NASA-CASE-GSC-12223-1
Filed 21 May 79 patented 12 Apr 83 15p
Languages: English Document Type: Patent
Journal Announcement: GRAI8320; STAR2114
Supersedes PAT-APPL-6-041 143, N79-27864 (17 - 18, p 2462).
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of patent available Commissioner of Patents, Washington, DC 20231, $1.00.
NTIS Prices: Not available NTIS
Country of Publication: United States
An apparatus for processing multidimensional data with strong spatial characteristics, such as raw image data, characterized by a large number of parallel data streams in an ordered array is described. It comprises a large number (e.g., 16,384 in a 128 x 128 array) of parallel processing elements operating simultaneously and independently on **single bit** slices of a corresponding array of incoming data streams under control of a single set of instructions. Each of the processing elements comprises a **bidirectional** data bus in communication with a register for storing **single bit** slices together with a random access memory unit and associated circuitry, including a binary counter/shift register device, for performing logical and arithmetical computations on the bit slices, and an I/O unit for interfacing the **bidirectional** data bus with the data stream source. The **massively parallel processor** architecture enables very high speed processing of large amounts of ordered parallel data, including spatial translation by shifting or sliding of bits **vertically** or **horizontally** to neighboring processing elements.
Descriptors: *Patents; *Architecture (Computers); *Computer design; *Parallel processing (Computers); Airborne/spaceborne computers; Image processing; Logical elements; Random access memory; Shift registers
Identifiers: PAT-CL-364-200; NTISGPNASA
Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware); 62B (Computers, Control, and Information Theory--Computer Software)

38/5/21 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

15193619 PASCAL No.: 01-0358816
Combined convective flow over a horizontal **cylinder in a porous medium near a** vertical **impermeable surface**
3rd European thermal sciences conference : Heidelberg, 10-13 September

2000
OOSTHUIZEN Patrick H
HAHNE EWP, ed; HEIDEMANN W, ed; SPINDLER K, ed
HEAT TRANSFER LABORATORY, Department of Mechanical Engineering, Queen's University, Kingston, Ontario, K7L 3N6, Canada
European thermal sciences conference, 3 (Heidelberg DEU) 2000-09-10
2000 473-478
Publisher: ETS, Pisa
ISBN: 88-467-0305-7 Availability: INIST-Y 33303; 354000092405250730
No. of Refs.: 17 ref.
Document Type: C (Conference Proceedings) ; A (Analytic)
Country of Publication: Italy
Language: English

A numerical study of laminar, two-dimensional combined (or mixed) convective flow over a circular cylinder embedded in a saturated porous medium has been numerically studied. The axis of a cylinder is in a **horizontal** plane and is arranged at right angles to the oncoming **vertical** forced flow. The cylinder is heated to a uniform surface temperature which is higher or lower than that of the fluid in the forced flow ahead of the cylinder. There is a **vertical** impermeable surface near the cylinder. This surface is at the temperature of liquid flowing over the cylinder. The study is based on the Darcy type assumptions with the buoyancy terms being treated using the Boussinesq approximation. The governing equations, written in dimensionless form, have been solved using the finite element method. The solution has as parameters the dimensionless distance, H, of the cylinder from the impermeable surface, the Peclet number, **Pe** , a buoyancy parameter, B, and depends on whether the buoyancy forces act in the same or in the **opposite direction** to the direction of the forced flow (i.e. on whether there is assisting or opposing flow). Results have been obtained for a range of values of the parameters for both assisting and opposing flows. The results indicate that the distance of the cylinder from the surface only has an effect on the heat transfer rate from the cylinder when the cylinder is very close to the surface or when the Peclet number is low.

English Descriptors: **Horizontal** cylinder; Buried pipe; Convection flow; Porous medium; Heat transfer; Nusselt number; Modeling

French Descriptors: Cylindre **horizontal** ; Canalisation enterree; Ecoulement convection; Milieu poreux; Transfert chaleur; Nombre Nusselt; Modelisation

Classification Codes: 001D06D02B; 230

Copyright (c) 2001 INIST-CNRS. All rights reserved.

38/5/22 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

12610341 PASCAL No.: 96-0298618
Circulation in the Alboran Sea as determined by quasi-synoptic hydrographic observations. Part II: Mesoscale ageostrophic motion diagnosed through density dynamical assimilation
VIUDEZ A; HANEY R L; TINTORE J
Departament de Fisica, Universitat de les Illes Balears, Palma de Mallorca, Spain
Journal: Journal of physical oceanography, 1996, 26 (5) 706-724
ISSN: 0022-3670 CODEN: JPYOBT Availability: INIST-15148;

354000043676380040
No. of Refs.: 1 p.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: United States
Language: English

The 3D velocity field in the Alboran Sea (Western Mediterranean) is diagnosed through density dynamical assimilation in a primitive equation (**PE**) model with mesoscale resolution. The ageostrophic motion is computed from fields produced by short-term backward and forward integrations of the **PE** model initialized with quasisynoptic CTD data. A weight function based on a low-pass digital filter (Digital Filter Initialization method) is applied to the resulting time series of model variables to obtain the final, dynamically balanced, density and 3D velocity fields. The diagnosed ageostrophic motion is interpreted by comparing the **vertical** velocity field with that obtained from the quasigeostrophic (QG) omega equation. The two methods produce very similar results with maximum **vertical** motions in the range of 10-20 m d SUP - SUP 1 associated with the differential advection of relative vorticity in small-scale jet meanders (upward (downward) motion upstream (downstream) of the ridges). Small local differences between **PE** and QG **vertical** velocities (typically 1-2 m d SUP - SUP 1) are attributed to known limitations of the QG theory and to differences between the analyzed and the dynamically initialized density fields. The **horizontal** ageostrophic motion in the western Alboran gyre (WAG) is in the same direction as the geostrophic motion above 100 m but in the **opposite direction** below 100 m. While the **horizontal** ageostrophic motion in the WAG can imply inflow or outflow depending on the position of local meanders, the gyre-scale ageostrophic circulation is characterized by convergence above 100 m and divergence below 100 m, implying an average downward motion of less than 1 m d SUP - SUP 1 . The general success of this assimilation approach could provide an alternative to QG diagnosis in mesoscale dynamics.

English Descriptors: Sea circulation; Data assimilation; Mesoscale; Three dimensional structure; Weight function; Digital filter; Time series; Density; Velocity distribution; Vortex motion; Alboran Sea; Advection; Vorticity; **Vertical** speed; Jet(atmosphere, ocean); Meander; **Vertical** motion
Broad Descriptors: Mediterranean Sea; Mer Mediterranee; Mar Mediterraneo

French Descriptors: Circulation marine; Assimilation donnee; Mesoechelle; Structure 3 dimensions; Fonction poids; Filtre numerique; Serie temporelle; Densite; Distribution vitesse; Mouvement tourbillon; Mer d'Alboran; Advection; Vorticite; Vitesse **verticale** ; Jet(atmosphere, ocean); Meandre; Mouvement **vertical**

Classification Codes: 001E02B05

38/5/23 (Item 1 from file: 434)
DIALOG(R)File 434:SciSearch(R) Cited Ref Sci
(c) 1998 Inst for Sci Info. All rts. reserv.

08334531 Genuine Article#: K0672 Number of References: 19
Title: A PARALLEL IMAGE SEGMENTATION ALGORITHM USING RELAXATION WITH VARYING NEIGHBORHOODS AND ITS MAPPING TO ARRAY PROCESSORS
Author(s): DERIN H; WON CS
Corporate Source: UNIV MASSACHUSETTS,DEPT ELECT & COMP ENGN/AMHERST//MA/01003
Journal: COMPUTER VISION GRAPHICS AND IMAGE PROCESSING, 1987, V40, N1, P 54-78

Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: COMPUTER APPLICATIONS & CYBERNETICS
Research Fronts: 86-8118 002 (DIGITAL ELEVATION MODELS; NOISY IMAGES; IMAGE-PROCESSING METHOD; IMAGE-ANALYSIS TECHNIQUES)
86-0032 001 (LONG-RANGE ISING SPIN-GLASSES; SPIN-GLASS TRANSITION; SK MODEL; DYNAMIC MEAN-FIELD THEORY; DZYALOSHINSKY-MORIYA ANISOTROPY IN REENTRANT ALLOYS)
86-0341 001 (PARALLEL PROCESSING; ROW-ORDERING SCHEMES FOR SPARSE GIVENS TRANSFORMATIONS; SYSTOLIC ARRAYS; QR FACTORIZATION; VLSI ALGORITHMS; HIGH-PERFORMANCE COMPUTERS)
86-1793 001 (PARALLEL PROCESSING SYSTEMS; INTERCONNECTION NETWORKS; VLSI ALGORITHM; MESH-CONNECTED **PROCESSOR ARRAY** ; DUAL SYSTOLIC ARCHITECTURES; PERFORMANCE ANALYSIS)
86-1887 001 (INCOMPLETE BLOCK-DESIGNS; EFFICIENCY FACTORS; **ROW - COLUMN** DESIGNS; VARIANCE **MODEL** ; FIELD EXPERIMENTS)
Cited References:
BESAG J, 1974, V36, P192, J ROY STAT SOC B MET
BESAG JE, 1986, COMMUNICATION APR
BESAG JE, 1983, 44TH SESS INT STAT I
COHEN FS, 1984, LEMS7 BROWN U LAB EN
CRISTI R, 1985, ISCS 85 JAPAN
DERIN H, 1984, V6, P707, IEEE T PATTERN ANAL
DERIN H, IN PRESS COMPUT VISI
DERIN H, IN PRESS IEEE T PATT
ELLIOTT H, 1984, 1984 P INT C ASSP SA
GEMAN S, 1984, V6, P721, IEEE T PATTERN ANAL
HANSEN FR, 1982, V20, P101, COMPUT GRAPHICS IMAG
KUNG HT, 1982, P37, IEEE COMPUTER JAN
LEVINE MD, 1985, V7, P155, IEEE T PATTERN ANAL
PRESTON K, 1983, V16, P36, COMPUT
ROSENFELD A, 1982, V1, DIGITAL PICTURE PROC
ROSENFELD A, 1982, V2, DIGITAL PICTURE PROC
ULLMAN JD, 1984, COMPUTATIONAL ASPECT
WON CS, 1986, THESIS U MASSACHUSET
YASNOFF WA, 1977, V9, P217, PATTERN RECOGNITION

38/5/24 (Item 2 from file: 434)
DIALOG(R)File 434:SciSearch(R) Cited Ref Sci
(c) 1998 Inst for Sci Info. All rts. reserv.

07595683 Genuine Article#: E5212 Number of References: 150
Title: A SURVEY OF STEPPING-STONE MODELS IN POPULATION-DYNAMICS
Author(s): RENSHAW E
Corporate Source: UNIV EDINBURGH,DEPT STAT,KINGS BLDG,MAYFIELD RD/EDINBURGH EH9 3JZ/MIDLOTHIAN/SCOTLAND/
Journal: ADVANCES IN APPLIED PROBABILITY, 1986, V18, N3, P581-627
Language: ENGLISH Document Type: REVIEW, BIBLIOGRAPHY
Geographic Location: SCOTLAND
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: STATISTICS & PROBABILITY
Research Fronts: 86-1178 004 (STATISTICAL DISTRIBUTION; SEQUENTIAL SAMPLING PLAN; CEREAL APHID POPULATIONS; SPATIAL PATTERN; FIELD CORN; DISPERSION PATTERNS)
86-5979 003 (CELL-CYCLE CONTROLS; DYNAMICS IN HIERARCHICALLY ORGANIZED SYSTEMS; NUCLEAR GROWTH DURING G1)
86-6825 003 (OPEN NETWORKS OF QUEUES; TELEPHONE NETWORK PERFORMANCE;

CLOSED QUEUING-NETWORKS; TANDEM CONFIGURATIONS; AGES OF ALLELES)
86-7933 002 (STRUCTURED POPULATIONS; BOUNDARY DYNAMICS; STEPPING-STONE MODELS IN POPULATION-DYNAMICS)
86-0564 001 (GENETIC DIFFERENTIATION; ELECTROPHORETIC ANALYSIS; BIOCHEMICAL SYSTEMATICS; GENETIC-VARIATION IN ALLOZYMES; GENETIC-DIVERGENCE AMONG POPULATIONS)
86-1300 001 (SUPERCRITICAL GALTON-WATSON PROCESS; BRANCHING-PROCESS MODEL; TIME RESPONSE OF THE STAIRCASE AVALANCHE PHOTODIODE; ASYMPTOTIC PROPERTIES)
86-1793 001 (PARALLEL PROCESSING SYSTEMS; INTERCONNECTION NETWORKS; VLSI ALGORITHM; MESH-CONNECTED **PROCESSOR ARRAY** ; DUAL SYSTOLIC ARCHITECTURES; PERFORMANCE ANALYSIS)
86-1887 001 (INCOMPLETE BLOCK-DESIGNS; EFFICIENCY FACTORS; **ROW - COLUMN** DESIGNS; VARIANCE **MODEL** ; FIELD EXPERIMENTS)
86-2434 001 (SPECIES AREA RELATIONSHIPS; ISLAND BIOGEOGRAPHY; INSULAR SMALL MAMMALS; RARITY IN PLANTS; HABITAT HETEROGENEITY; FOREST BIRDS; BIRD COMMUNITIES)
86-2767 001 (BROWNIAN EXCURSIONS; COMPLEX BROWNIAN-MOTION; PERCOLATION IN RANDOM-FIELDS; ONE-DIMENSIONAL DIFFUSIONS; MULTIPLE POINTS; 2 INTERACTING SYSTEMS)
86-3428 001 (INTRACELLULAR PATTERN REVERSAL; CHICK LIMB BUDS; MECHANICAL MODEL FOR BIOLOGICAL PATTERN-FORMATION; POSITIONAL SYSTEM; CELL PATTERNING; EARLY DEVELOPMENT)
86-4203 001 (SPATIAL MODELS; RANDOM ASSOCIATION; DISEASE SEVERITY DATA)

Cited References:

ABRAMOWITZ M, 1965, V55, AMS US DEP COMMERCE
ADKE SR, 1969, V6, P687, J APPL PROBAB
ADKE SR, 1964, V2, P32, J IND STATIST ASS
ADKE SR, 1963, V7, P209, J MATH ANAL APPL
ADKE SR, 1964, V9, P336, J MATH ANAL APPL
AKSLAND M, 1975, V7, P44, ADV APPL PROB
ANDERSON RM, 1982, POPULATION DYNAMICS
ARLEY N, 1945, V76, P261, ACTA MATH
ARMITAGE P, 1952, V14, P1, J ROY STAT SOC B MET
ARNASON AN, 1971, THESIS U EDINBURGH
ARNOLD L, 1974, STOCHASTIC DIFFERENT
BAILEY NTJ, 1968, V55, P189, BIOMETRIKA
BAILEY NTJ, 1975, MATH THEORY INFECTIO
BAILEY NTJ, 1967, V4, P237, 5TH P BERK S MATH ST
BARTHOLOMEW DJ, 1967, STOCHASTIC MODELS SO
BARTLETT MS, 1957, V44, P27, BIOMETRIKA
BARTLETT MS, 1949, V11, P211, J ROY STAT SOC B MET
BARTLETT MS, 1960, STOCHASTIC POPULATIO
BARTLETT MS, 1956, V4, P81, 3RD P BERK S MATH ST
BENES VE, 1965, MATH THEORY CONNECTI
BRAMSON M, 1983, V44, P1, MEM AM MATH SOC
BROADBENT R, 1953, V9, P460, BIOMETRICS
CHEWNING WC, 1975, V23, P253, MATH BIOSCI
CHIANG CL, 1968, INTRO STOCHASTIC PRO
CHIANG CL, 1980, INTRO STOCHASTIC PRO
CLIFF AD, 1981, SPATIAL DIFFUSION HI
COX DR, 1957, V44, P328, BIOMETRIKA
COX DR, 1965, THEORY STOCHASTIC PR
CRUMP KS, 1970, V7, P565, J APPL PROBAB
DANIELS HE, 1977, V14, P689, J APPL PROBAB
DANIELS HE, 1975, P373, PERSPECTIVES PROBABI
DAVIS AW, 1970, V2, P83, ADV APPL PROB
DAVIS AW, 1965, V2, P293, J APPL PROBAB
DAVIS AW, 1967, V18, P276, J MATH ANAL APPL
DAVIS AW, 1967, V19, P1, J MATH ANAL APPL
DUBOIS DM, 1978, V78, P384, COMPSTAT

DUBOIS DM, 1975, V1, P67, ECOL MODEL
DURRETT R, 1979, V9, P117, STOCH P APPL
DURRETT R, 1981, V11, P109, STOCHASTIC PROCESS A
FADDY MJ, 1977, V9, P448, ADV APPLIED PROBABIL
FADDY MJ, 1980, V17, P839, J APPL PROBAB
FADDY MJ, 1983, V20, P715, J APPL PROBAB
FELLER W, 1939, V5, P11, ACTA BIOTHEORET
FISHER RA, 1937, V7, P355, ANN EUGEN
FLEMING WH, 1974, V5, P431, THEOR POPUL BIOL
GANI J, 1962, V49, P272, BIOMETRIKA
GANI J, 1965, V2, P150, J APPL PROBAB
GANI J, 1965, V2, P225, J APPL PROBAB
GANI J, 1962, V2, P478, J AUSTR MATH SOC
GANS PJ, 1960, V33, P691, J CHEM PHYS
GRIFFEATH D, 1981, V11, P151, STOCHASTIC PROCESS A
GRIFFITHS DA, 1972, V9, P65, J APPL PROBAB
GRIFFITHS DA, 1973, V10, P15, J APPL PROBAB
HARRIS TE, 1963, THEORY BRANCHING PRO
HELLIWELL DR, 1975, V7, P61, BIOL CONSERVATION
HOLGATE P, 1968, V5, P1, J APPL PROBAB
HORN HS, 1972, V53, P749, ECOLOGY
HUFFAKER CB, 1958, V27, P343, HILGARDIA
ITATSU S, 1981, V83, P37, NAGOYA MATH J
JACKSON JR, 1957, V5, P518, OPER RES
JERNIGAN RW, 1980, V10, P1, ECOL MOD
KARLIN S, 1957, V85, P489, T AM MATH SOC
KARLIN S, 1957, V86, P366, T AM MATH SOC
KELKER D, 1973, V68, P821, J AM STAT ASSOC
KELLY FP, 1979, REVERSIBILITY STOCHA
KENDALL DG, 1948, V19, P1, ANN MATH STAT
KENDALL DG, 1948, V35, P316, BIOMETRIKA
KENDALL DG, 1965, P213, MATH COMPUTER SCI BI
KENYON EA, 1982, THESIS U EDINBURGH
KIMURA M, 1953, V3, P62, ANNU REP NAT I GENET
KIMURA M, 1963, V17, P279, EVOLUTION
KIMURA M, 1964, V49, P561, GENETICS
KINGMAN JFC, 1969, V6, P1, J APPL PROBAB
KOLMOGOROFF AN, 1937, V1, P1, B STATE U MOSCOW A
KRIEGER IM, 1960, V32, P247, J CHEM PHYS
KUULASMAA K, 1982, V19, P745, J APPL PROBAB
LESLIE PH, 1958, V45, P316, BIOMETRIKA
LEVIN SA, 1974, V108, P207, AM NAT
LEVIN SA, 1978, V2, P439, MATH ASS AM STUDY MA
LEVINS R, 1971, V68, P1246, P NATL ACAD SCI USA
LIGGETT TM, 1985, INTERACTING PARTICLE
LIGGETT TM, 1973, V179, P433, T AM MATH SOC
LIGGETT TM, 1974, V198, P201, T AM MATH SOC
LOTKA AJ, 1925, ELEMENTS PHYSICAL BI
MACARTHUR R, 1967, THEORY ISLAND BIOGEO
MARUYAMA T, 1970, V2, P229, ADV APPL PROB
MARUYAMA T, 1969, V6, P463, J APPL PROBAB
MATIS JH, 1971, V27, P77, BIOMETRICS
MILCH PR, 1968, V39, P727, ANN MATH STAT
MIMURA M, 1978, V75, P249, J THEOR BIOL
MODE CJ, 1962, V18, P543, BIOMETRICS
MODE CJ, 1971, V10, P177, MATH BIOSCI
MODE CJ, 1971, MULTITYPE BRANCHING
MOLLISON D, 1972, V4, P233, ADV APPL PROB
MOLLISON D, 1977, V39, P283, J ROY STAT SOC B MET
MOLLISON D, 1972, V3, P579, 6TH P BERK S MATH ST
MORGAN BJT, 1976, V13, P672, J APPL PROBAB

MORGAN RW, 1965, V27, P497, J R STATISTIC SOC B
NEYMAN J, 1957, V22, P109, COLD SPRING HARB SYM
NEYMAN J, 1956, V4, P41, 3 P BERK S MATH STAT
NISBET RM, 1982, MODELLING FLUCTUATIN
NOTOHARA M, 1980, V10, P281, J MATH BIOL
OKUBO A, 1980, DIFFUSION ECOLOGICAL
PATIL VT, 1957, V44, P43, BIOMETRIKA
PURI PS, 1968, V5, P334, J APPL PROBAB
RADCLIFFE J, 1969, V6, P186, J APPL PROBAB
RAMAN S, 1973, V10, P718, J APPL PROBAB
REID WT, 1959, V8, P221, J MATH MECH
RENSHAW E, 1972, V59, P49, BIOMETRIKA
RENSHAW E, 1973, V10, P1, J APPL PROBAB
RENSHAW E, 1974, V11, P16, J APPL PROBAB
RENSHAW E, 1977, V14, P591, J APPL PROBAB
RENSHAW E, 1979, V16, P1, J APPL PROBAB
RENSHAW E, 1980, V17, P895, J APPL PROBAB
RENSHAW E, 1981, V18, P715, J APPL PROBAB
RENSHAW E, 1982, V94, P355, J THEOR BIOL
RENSHAW E, 1976, THESIS U EDINBURGH
RENSHAW E, 1973, V2, P294, 39TH P SESS INT STAT
RUBEN H, 1962, V33, P119, ANN MATH STAT
RUSHTON S, 1955, V42, P126, BIOMETRIKA
SAWYER S, 1977, V9, P268, ADV APPL PROBABILITY
SAWYER S, 1976, V4, P699, ANN PROBAB
SAWYER S, 1983, V20, P1, J APPL PROBAB
SEVERO NC, 1967, V4, P271, J APPL PROBAB
SEVERO NC, 1969, V6, P673, J APPL PROBAB
SHERMAN B, 1958, V29, P267, ANN MATH STAT
SHERMAN B, 1956, 60946983P3 WEST RES
SHIGA T, 1980, V20, P212, J MATH KYOTO U
SHIGA T, 1980, V20, P723, J MATH KYOTO U
SHIGA T, 1982, V22, P1, J MATH KYOTO U
SHIGA T, 1985, POPULATION GENETICS
SIEGERT AJF, 1949, V76, P1708, PHYS REV
SKELLAM JG, 1951, V38, P196, BIOMETRIKA
SMITH JM, 1974, MODELS ECOLOGY
SMITH RH, 1979, V80, P189, J THEOR BIOL
SPITZER F, 1970, V5, P246, ADV MATH
TALLIS GM, 1966, V22, P409, BIOMETRICS
TURING AM, 1952, V237, P37, PHIL T ROY SOC LON B
UCHIYAMA K, 1982, V10, P896, ANN PROBAB
UCHIYAMA K, 1978, V18, P453, J MATH KYOTO U
UCHIYAMA K, 1981, V57, P90, P JPN ACAD A-MATH
USHER MB, 1970, V23, P1, BIOMETRICS
VANDERMEER JH, 1973, V41, P161, J THEOR BIOL
VOLTERRA V, 1931, LECONS THEORIE MATH
WEISS GH, 1965, V2, P129, J APPL PROBAB
WHITTLE P, 1954, V41, P434, BIOMETRIKA
WHITTLE P, 1968, V5, P567, J APPL PROBABIL
WHITTLE P, 1967, V2, P642, 36TH P SESS INT STAT
WIGGINS AD, 1960, V16, P642, BIOMETRICS
WRIGHT S, 1943, V28, P114, GENETICS

38/5/25 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

07255046 Genuine Article#: 142VC Number of References: 17

Title: An efficient method for approximating submesh reliability of

two-dimensional meshes
Author(s): Chang CY (REPRINT) ; Mohapatra P
Corporate Source: AMDAHL CORP,1250 E ARQUES AVE/SUNNYVALE//CA/94088 (REPRINT); IOWA STATE UNIV SCI & TECHNOL,DEPT ELECT & COMP ENGN/AMES//IA/50011
Journal: IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, 1998, V9, N11 (NOV), P1115-1124
ISSN: 1045-9219 Publication date: 19981100
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Geographic Location: USA
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, THEORY & METHODS
Abstract: An analytical model for submesh reliability of mesh-connected systems is proposed in this paper. A mesh is considered operational as long as a functional submesh of the required size is available. We use the principle of inclusion and exclusion to find the exact probability of having a functional submesh within a partition of the mesh. The partitions are taken along either dimension of the mesh. The partitions along the rows are called row partitions (RPs) and along the columns are called column partitions (CPs). The reliability of a partition is then used to approximate the submesh reliability of the system and, thus, this model is called partitioned mesh (PM) model. Instead of using a computationally intensive recursive algorithm as done in the previous work, a closed form approximation of the submesh reliability is derived in this paper. The PM model is validated through simulation and compared with the earlier proposed approximation techniques. It is shown that the PM model provides better approximations for submesh reliability with constant computational complexity.
Descriptors--Author Keywords: **column** partition ; partitioned mesh **model** ; **row** partition ; submesh reliability ; two-dimensional mesh
Identifiers--KeyWord Plus(R): **PROCESSOR ARRAYS** ; ALLOCATION
Cited References:
BOEHME TK, 1992, P451, IEEE T RELIABILI SEP
CHANG YK, 1995, V44, P952, IEEE T COMPUT
CHEAN M, 1990, P55, COMPUTER
CHUANG PJ, 1994, P211, IEEE T PARALLEL FEB
COUVILLION JA, 1991, V8, P69, IEEE SOFTWARE
DERMAN C, 1982, P57, IEEE T RELIABILI APR
DING J, 1993, V2, P193, P INT C PARALLEL PRO
FORTES JAB, 1985, V34, P1033, IEEE T COMPUT
HWANG K, 1993, ADV COMPUTER ARCHITE
LAM CWH, 1989, V38, P833, IEEE T COMPUT
LI K, 1991, P413, IEEE T PARALL DISTR
LI KQ, 1991, V12, P79, J PARALLEL DISTR COM
LOPEZBENITEZ N, 1992, V41, P1193, IEEE T COMPUT
MOHAPATRA P, 1995, V44, P1073, IEEE T COMPUT
SAHNER R, 1987, P186, IEEE T RELIAB
SALVIA AA, 1990, V39, P382, IEEE T RELIAB
ZHU YH, 1992, V16, P328, J PARALLEL DISTR COM

38/5/26 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

03435126 Genuine Article#: PD793 Number of References: 42
Title: A HIGHLY OR-PARALLEL INFERENCE MACHINE (MULTI-ASCA) AND ITS PERFORMANCE EVALUATION - AN ARCHITECTURE AND ITS LOAD BALANCING

ALGORITHMS
Author(s): NAGANUMA J; OGURA T
Corporate Source: NIPPON TELEGRAPH & TEL PUBL CORP,LSI LABS,3-1 MORINOSATO WAKAMIYA/ATSUGI/KANAGAWA 24301/JAPAN/
Journal: IEEE TRANSACTIONS ON COMPUTERS, 1994, V43, N9 (SEP), P1062-1075
ISSN: 0018-9340
Language: ENGLISH Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, HARDWARE & ARCHITECTURE
Abstract: An architecture and its four load balancing algorithms for a highly OR-parallel inference machine are proposed, and its performance is evaluated in a trace-driven simulation study. This inference machine consists of a large number of processing elements (**PE** 's) with **serial** I/O **links** directly connected to each other in a simply modified mesh network. Each **PE** is a high-speed sequential Prolog processor with its own local memory. The activity of all **PE** 's is locally controlled by four new load balancing algorithms based on purely local communication. Communication is allowed only between directly connected **PE** 's. These load balancing algorithms reduce communication overhead in a load balancing and make it possible to accomplish highly OR-parallel execution. A software simulator using a trace-driven simulation technique based on an inference tree has been developed, and some typical OR-parallel benchmarks such as the n-queens problem have been simulated on it. The average communication per load balancing is reduced by a factor ranging from 1/30 to 1/100 by the interaction of these load balancing algorithms as compared with a conventional copying method. The inference machine (1024 **PE** 's: 32 x 32 array) attains 300-600 times parallel speedup, assuming 1 MLIPS (mega logical inference per second) **PE** and a 20 MBPS (mega bit per second) each **serial** I/O **link** , which could be easily integrated on a single chip using current VLSI technology. This highly OR-parallel inference machine promises to be an important step towards the realization of a high-performance artificial intelligence system.
Descriptors--Author Keywords: HIGHLY PARALLEL INFERENCE MACHINE ARCHITECTURE ; LOAD BALANCING ALGORITHMS ; LOGIC PROGRAMMING LANGUAGE ; NONSHARED MEMORY MULTIPROCESSOR SYSTEM ; OR-PARALLEL EXECUTION ; PERFORMANCE EVALUATION ; PROLOG ; TRACE DRIVEN SIMULATION
Identifiers--KeyWords Plus: PROLOG
Research Fronts: 92-1723 003 (OBJECT-ORIENTED LOGIC PROGRAMMING SYSTEM; LINEAR RECURSIVE QUERIES IN DEDUCTIVE DATABASES; ARCHITECTURAL SUPPORT FOR GOAL MANAGEMENT)
92-1105 001 (LOGIC PROGRAMS; QUALITATIVE MODEL-BASED INTELLIGENT CONTROL OF A DISTILLATION **COLUMN** ; ABDUCTION IN LEARNING DIAGNOSTIC KNOWLEDGE)
Cited References:
ALI K, 1988, P1531, 5TH P INT C S LOG PR
ALI KAM, 1987, V15, P189, INT J PARALLEL PROG
ALI KAM, 1990, V19, P129, INT J PARALLEL PROG
ALI KAM, 1992, P739, JUN P INT C FGCS 92
ALI KAM, 1991, P807, 1991 P INT C LOG PRO
ALSHAWI H, 1988, P1578, 1988 P INT C LOG PRO
BARON U, 1988, P841, NOV P INT C FGCS 88
BORGWARDT P, 1984, P2, 1984 P S LOG PROGR
CALDERWOOD A, 1989, P419, 6TH P INT C LOG PROG
CARLSSON M, 1990, SICSTUS PROLOG USERS
CHENG PS, 1969, V8, P280, IBM SYST J
CIEPIELEWSKI A, 1991, V20, P421, INT J PARALLEL PROG
CLOCKSIN WF, 1987, V30, P386, COMPUT J

CLOCKSIN WF, 1981, PROGRAMMING PROLOG
CONERY JS, 1981, P163, OCT P ACM C FUNCT LA
CRAMMOND J, 1985, V34, P911, IEEE T COMPUT
DORBY TP, 1985, P180, 12TH P ANN S COMP AR
KAI M, 1988, V29, P647, T INFORM PROCESSING
KAWAGUCHI T, 1992, V75, P380, T IEICE JAPAN
KERNIGHAN BW, 1978, C PROGRAMMING LANGUA
KOWALSKI RA, 1979, LOGIC PROBLEM SOLVIN
LUSK E, 1988, P819, NOV P INT C FGCS 88
MAY D, 1992, P209, 1992 P IEEE INT C CO
NAGANUMA J, 1988, V37, P1375, IEEE T COMPUT
NAGANUMA J, 1989, OCT P ICOT PIM WG WO
NAGANUMA J, 1990, V73, P856, T IEICE JAPAN
NAGANUMA J, 1991, P229, 14TH P ANN HAW INT C
NAGANUMA J, 1987, P201, 34TH P ANN C IPS
NAGANUMA J, 1987, P137, 35TH P ANN C IPS
NAKASHIMA H, 1990, P355, 1990 P IEEE INT C CO
OGURA T, 1985, V20, P1277, IEEE J SOLID-ST CIRC
SARASWAT KC, 1982, V29, P645, IEEE T ELECTRON DEV
SHAPIRO EY, 1987, CONCURRENT PROLOG CO
SHAPIRO EY, 1987, P311, 1987 P INT C LOG PRO
SOHMA Y, 1986, P3, NEW PARALLEL INFEREN
STERLING L, 1986, ART PROLOG PROGRAMMI
TAMAKI H, 1988, P287, 4TH SOFTW SCI JAP TE
TICK E, 1984, P29, 1984 P INT S LOG PRO
UCHIDA S, 1992, P33, JUN P INT C FGCS 92
WARREN DHD, 1987, P92, 1987 P INT S LOG PRO
WARREN DHD, 1983, 309 SRI INT TECHN NO
WESTPHAL H, 1987, P436, 1987 P S LOG PROGR

38/5/27 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

02665656 Genuine Article#: LV291 Number of References: 30
Title: NUCLEAR-MAGNETIC-RESONANCE IMAGING OF MISCIBLE FINGERING IN POROUS-MEDIA
Author(s): PEARL Z; MAGARITZ M; BENDEL P
Corporate Source: WEIZMANN INST SCI,DEPT ENVIRONM SCI & ENERGY RES/IL-76100 REHOVOT//ISRAEL/; WEIZMANN INST SCI,DEPT CHEM PHYS/IL-76100 REHOVOT//ISRAEL/
Journal: TRANSPORT IN POROUS MEDIA, 1993, V12, N2 (AUG), P107-123
ISSN: 0169-3913
Language: ENGLISH Document Type: ARTICLE
Geographic Location: ISRAEL
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, CHEMICAL
Abstract: Nuclear Magnetic Resonance Imaging (MRI) can noninvasively map the spatial distribution of Nuclear Magnetic Resonance (NMR)-sensitive nuclei. This can be utilized to investigate the transport of fluids (and solute molecules) in three-dimensional model systems. In this study, MRI was applied to the buoyancy-driven transport of aqueous solutions, across an unstable interface in a three-dimensional box model in the limit of a small Peclet number (**Pe** <0.4). It is demonstrated that MRI is capable of distinguishing between convective transport ('fingering') and molecular diffusion and is able to quantify these processes. The results indicate that for homogeneous porous media, the total fluid volume displaced through the interface and the amplitude of the fastest growing finger are linearly correlated with

time. These linear relations yielded mean and maximal displacement velocities which are related by a constant dimensionless value (2.4+/-0.1). The mean displacement velocity (U) allows us to calculate the media permeability which was consistent between experiments (1.4+/-0.1 x 10(-7) cm2). U is linearly correlated with the initial density gradient, as predicted by theory. An extrapolation of the density gradient to zero velocity enables an approximate determination of the critical density gradient for the onset of instability in our system (0.9+/-0.3 x 10(-3) g/cm3), a value consistent with the value predicted by a calculation based upon the modified Rayleigh number. These results suggest that MRI can be used to study complex fluid patterns in three-dimensional box models, offering a greater flexibility for the simulation of natural conditions than conventional experimental modelling methods.

Descriptors--Author Keywords: NUCLEAR MAGNETIC RESONANCE IMAGING (MRI) ; MISCIBLE DISPLACEMENT ; BUOYANCY ; 3-DIMENSIONAL ; DIFFUSION ; PERMEABILITY

Identifiers--KeyWords Plus: WATER; DIFFUSION; FLOW

Research Fronts: 91-2091 001 (SOLUTE TRANSPORT IN GROUNDWATER; UNSATURATED FLOW THEORY; SATURATED SOILS)

91-2355 001 (DIRECTIONAL SOLIDIFICATION; SELF-DILATING VISCOUS FINGERS IN WEDGE-SHAPED HELE-SHAW CELLS; CELLULAR GROWTH; PATTERN SELECTION; 2-DIMENSIONAL INTERFACE)

91-3996 001 (MIXED CONVECTION IN POROUS-MEDIA; HOT FLUID MIGRATION; THERMAL REGIME; HEAT-FLOW **MODELING** ; **HORIZONTAL** PLATE; **VERTICAL** SURFACES)

91-5115 001 (NMR IMAGING OF WATER; NUCLEAR-MAGNETIC-RESONANCE MICROSCOPY; STRUCTURE IN CONCENTRATED SUSPENSIONS)

Cited References:

BALDWIN BA, 1988, V6, P493, MAGN RESON IMAGING
BEAR J, 1972, DYNAMICS FLUIDS PORO
BEAR J, 1979, HYDRAULICS GROUNDWAT
BENDEL P, 1990, V86, P509, J MAGN RESON
BUDINGER TF, 1984, V226, P288, SCIENCE
CARRINGTON A, 1979, CH13, INTRO MAGNETIC RESON
CHEN JD, 1988, V61, P1489, PHYS REV LETT
COSKUNER G, 1990, V5, P473, TRANSPORT POROUS MED
EDELSTEIN WA, 1979, SPE18272
EDELSTEIN WA, 1988, 63RD ANN TECHN C EXH
FREEZE RA, 1979, GROUNDWATER
GAIGALAS AK, 1989, V84, P113, NUCL TECHNOL
GUILLOT G, 1989, V22, P1846, J PHYS D
GUILLOT G, 1991, V24, P763, J PHYS D APPL PHYS
GUMMERSON RJ, 1979, V281, P56, NATURE
HALL LD, 1987, V74, P139, J MAGN RESON
HELLSTROM G, 1988, V24, P493, WATER RESOUR RES
HOMSY GM, 1987, V19, P271, ANNU REV FLUID MECH
IMNHOFF PT, 1988, V188, P363, J FLUID MECH
JEZZARD P, 1991, V23, P1, PROG NUCL MAG RES SP
KYLE CR, 1965, V5, P189, SOC PET ENG J
LAPWOOD ER, 1948, V44, P508, P CAMBRIDGE PHIL SOC
MOLZ FJ, 1983, V19, P149, WATER RESOUR RES
MORRIS PG, 1986, NUCLEAR MAGNETIC RES
OGER L, 1987, V4, P301, EUROPHYS LETT
PEARL Z, 1991, V95, P597, J MAGN RESON
RONEN D, 1988, V24, P1111, WATER RESOUR RES
WOODING RA, 1963, V15, P527, J FLUID MECH
WOODING RA, 1964, V19, P103, J FLUID MECH
WOODING RA, 1969, V39, P477, J FLUID MECH

38/5/28 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2002 Inst for Sci Info. All rts. reserv.

02427448 Genuine Article#: LA335 Number of References: 16
Title: MIXED CONVECTION ALONG A NONISOTHERMAL VERTICAL FLAT-PLATE EMBEDDED IN A POROUS-MEDIUM - THE ENTIRE REGIME
Author(s): HSIEH JC; CHEN TS; ARMALY BF
Corporate Source: UNIV MISSOURI,DEPT MECH & AEROSP ENGN & ENGN MECH/ROLLA//MO/65401
Journal: INTERNATIONAL JOURNAL OF HEAT AND MASS TRANSFER, 1993, V36, N7 (MAY), P1819-1825
ISSN: 0017-9310
Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: MECHANICS; ENGINEERING, MECHANICAL
Abstract: The problem of mixed convection about a vertical flat plate embedded in a porous medium is analyzed. Nonsimilarity solutions are obtained for the cases of variable wall temperature (VWT) in the form T(w)(x) = T(infinity) + ax(n) and variable surface heat flux (VHF) in the form q(w)(x) = bx(m). The entire mixed convection regime is covered by two different nonsimilarity parameters chi = [I + (Ra(x)/ **Pe** (x))1/2]-1 and chi* = [1 + (Ra(x)*/ **Pe** (x)3/2)1/3]-1, respectively, for VWT and VHF cases, from pure forced convection (chi = 1 or chi* = 1) to pure free convection (chi = 0 or chi* = 0). A finite-difference scheme was used to solve the system of transformed governing equations. Velocity and temperature profiles, and local Nusselt numbers are presented. It is found that as chi or chi* decreases from 1 to 0, the thermal boundary layer thickness increases first and then decreases, but the local Nusselt number in the form Nu(x)(**Pe** (x)1/2 + Ra(x)1/2)-1 or Nu(x)(**Pe** (x)1/2 + Ra(x)*1/3)-1 decreases first and then increases. The correlation equations for the local and average Nusselt numbers are also obtained for the two surface heating conditions.
Identifiers--KeyWords Plus: NATURAL-CONVECTION; SIMILARITY TRANSFORMATION; SURFACES; CYLINDER; FLOWS
Research Fronts: 91-3996 001 (MIXED CONVECTION IN POROUS-MEDIA; HOT FLUID MIGRATION; THERMAL REGIME; HEAT-FLOW **MODELING** ; **HORIZONTAL** PLATE; **VERTICAL** SURFACES)
Cited References:
BEJAN A, 1984, P355, CONVECTION HEAT TRAN
BEJAN A, 1984, V27, P717, INT J HEAT MASS TRAN
CEBECI T, 1977, CH7, MOMENTUM TRANSFER BO
CHENG P, 1976, V19, P1267, INT J HEAT MASS TRAN
CHENG P, 1977, V20, P893, INT J HEAT MASS TRAN
CHENG P, 1977, V20, P807, INT J HEAT MASS TRAN
CHENG P, 1977, V82, P2040, J GEOPHYS RES
CHENG P, 1981, V8, P261, LETT HEAT MASS TRANS
CHURCHILL SW, 1977, V23, P10, AICHE J
HONG JT, 1987, V109, P356, J HEAT TRANS-T ASME
HSIEH JC, 1993, V36, P1485, INT J HEAT MASS TRAN
HSU CT, 1985, V28, P683, INT J HEAT MASS TRAN
MINKOWYCZ WJ, 1976, V19, P805, INT J HEAT MASS TRAN
MINKOWYCZ WJ, 1985, V8, P349, NUMER HEAT TRANSFER
NAKAYAMA A, 1991, V34, P357, INT J HEAT MASS TRAN
NAKAYAMA A, 1987, V109, P1041, J HEAT TRANS-T ASME

38/5/29 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

(c) 2002 Inst for Sci Info. All rts. reserv.

02369544 Genuine Article#: KX210 Number of References: 10

Title: NONSIMILARITY SOLUTIONS FOR MIXED CONVECTION FROM VERTICAL SURFACES IN POROUS-MEDIA - VARIABLE SURFACE-TEMPERATURE OF HEAT-FLUX

Author(s): HSIEH JC; CHEN TS; ARMALY BF
Corporate Source: UNIV MISSOURI,DEPT MECH & AEROSP ENGN & ENGN MECH/ROLLA//MO/65401

Journal: INTERNATIONAL JOURNAL OF HEAT AND MASS TRANSFER, 1993, V36, N6 (APR), P1485-1493
ISSN: 0017-9310
Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: MECHANICS; ENGINEERING, MECHANICAL

Abstract: Nonsimilarity solutions for mixed convection from a vertical flat plate embedded in a porous medium are reported for two surface heating conditions: variable wall temperature (VWT) and variable surface heat flux (VHF) of the power-law form. The entire mixed convection regime is divided into two regions. One region covers the forced convection dominated regime and the other one covers the free convection dominated regime. The governing equations are first transformed into a dimensionless form by the nonsimilar transformation and then solved by a finite-difference scheme. Four nonsimilarity parameters are introduced. The parameters Ra(x)*/ **Pe** (x) and Ra(x)*/ **Pe** (x)3/2 characterize the effect of buoyancy forces on the forced convection for the VWT and VHF cases, respectively; while the parameters **Pe** (x)/Ra(x) and **Pe** (x)/Ra(x)*2/3 characterize the effect of forced flow on the free convection for VWT and VHF cases, respectively. Numerical results for both heating conditions are presented. Correlation equations for the local and average Nusselt numbers are also presented.

Identifiers--KeyWords Plus: CYLINDER
Research Fronts: 91-3996 001 (MIXED CONVECTION IN POROUS-MEDIA; HOT FLUID MIGRATION; THERMAL REGIME; HEAT-FLOW **MODELING** ; **HORIZONTAL** PLATE; **VERTICAL** SURFACES)

Cited References:
ALDOSS TK, 1993, V36, P463, INT J HEAT MASS TRAN
ALDOSS TK, 1993, V36, P471, INT J HEAT MASS TRAN
CEBECI T, 1977, CH7, MOMENTUM TRANSFER BO
CHENG P, 1977, V82, P2040, J GEOPHYS RES
CHENG P, 1981, V8, P261, LETT HEAT MASS TRANS
CHURCHILL SW, 1977, V23, P10, AICHE J
HONG JT, 1987, V109, P356, J HEAT TRANS-T ASME
MINKOWYCZ WJ, 1985, V8, P349, NUMER HEAT TRANSFER
RANGANATHAN P, 1984, V7, P305, NUMER HEAT TRANSFER
YUCEL A, 1984, V7, P483, NUMER HEAT TRANSFER

Search report

Set	Items	Description
S1	33994	MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCESSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGEMENT? OR ORDER OR FORMATION)
S2	16451	(SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N)(CONNECT? OR LINK?) OR SINGLE()BIT
S3	6608	MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?)
S4	8999	MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5	833	MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6	245	VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7	596022	VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8	648941	HORIZONTAL? OR ROW OR NORMAL?
S9	48828	BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE
S10	0	S1 (S) S2 (S) S3 (S) S4 (S) S5
S11	25	S1 (S) S2
S12	50360	S1 OR S2
S13	0	S12 (S) S3 (S) S4 (S) S5
S14	5	S12 (S) S3
S15	35	S12 (S) S4
S16	0	S15 (S) S5
S17	0	S12 (S) S6
S18	493	S12 (S) S7
S19	107	S18 (S) S8
S20	1	S19 (S) S9
S21	3	S18 (S) S9
S22	1	S18 (S) S7 (S) S8 (S) S9
S23	43	S14 OR S15 OR S20 OR S21 OR S22
S24	43	S23 NOT PY>2000
S25	43	S24 NOT PD>20000831
S26	32	RD (unique items)

File 275:Gale Group Computer DB(TM) 1983-2002/Jul 30
(c) 2002 The Gale Group
File 47:Gale Group Magazine DB(TM) 1959-2002/Jul 30
(c) 2002 The Gale group
File 75:TGG Management Contents(R) 86-2002/Jul W2
(c) 2002 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2002/Jul 30
(c) 2002 The Gale Group
File 16:Gale Group PROMT(R) 1990-2002/Jul 30
(c) 2002 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group

26/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

02083966 SUPPLIER NUMBER: 17800143 (USE FORMAT 7 OR 9 FOR FULL TEXT)
HP DeskJet 850C; HP DeskJet 340. (desktop and portable inkjet printers) (Hardware Review) (Evaluation)
Bojorquez, Tony A.
MacUser, v12, n3, p55(2)
March, 1996
DOCUMENT TYPE: Evaluation ISSN: 0884-0997 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1221 LINE COUNT: 00102

... an interruption.
The DeskJet 850C prints either over a LocalTalk connection--for network use--or via a **serial connection** . It's also equipped with a parallel port, which means you can connect both a Mac and a PC to the printer simultaneously. For setting print quality, you can choose one of three print **modes** (Econofast, **Normal** , and Best) with the software. HP's ColorSmart technology is an added plus--it lets the printer...

26/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01949302 SUPPLIER NUMBER: 18385311 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Axil's S/420 HyperSPARC server. (Axil Computer Inc file server) (Hardware Review) (Evaluation)
Barker, Ralph
UNIX Review, v14, n8, p53(5)
July, 1996
DOCUMENT TYPE: Evaluation ISSN: 0742-3136 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2802 LINE COUNT: 00228

... controller in the subsystem, along with associated configuration utilities. Earlier models of the S/420 provide a **serial** communication **link** between the main chassis and the RAID subsystem. To configure the RAID subsystem, the installer uses the...

...RAID level 5 is the desired configuration, the installed disks can be formatted and mounted in the **normal** manner. Newer **models** of the S/420 provide a utility that configures the subsystem directly via the SCSI bus.
Documentation...

26/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01890677 SUPPLIER NUMBER: 17488771 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Internetwork 1995 TCP/IP software directory. (Internetwork supplement) (includes company index) (Buyers Guide)
INTERNETWORK, v6, n8, pA1(20)
August, 1995
DOCUMENT TYPE: Buyers Guide LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 14920 LINE COUNT: 01298

... terminal. It supports DECnet, TCP/)P, Novell's NCSI communications server protocol, Netware for DEC Access and **serial connections** . A Winsock-compliant FTP client is also included. Advanced features include programmable toolbars, DDE support, 48 line display, 1 32 **column** display, a **modem** dialer, graphical keyboard mapper, command language and Xmodem, Ymodem, Zmodem and sliding windows Kermit file transfer. The...

26/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01826377 SUPPLIER NUMBER: 17372648 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Apple Color StyleWriter 2400 and 2200 and HP DeskWriter 660C: new crop of razzle-dazzle color inkjet printers. (Hardware Review)(Evaluation)
Bojorquez, Tony
MacUser, v11, n10, p49(2)
Oct, 1995
DOCUMENT TYPE: Evaluation ISSN: 0884-0997 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1430 LINE COUNT: 00118

...ABSTRACT: DeskWriter 660C uses separate black and three-color ink cartridges and comes with 27 TrueType fonts and **serial** and LocalTalk **connections** . Black text and line art prints at up to 600 by 600 dpi and best-quality color at 600 by 300 dpi; the ' **normal** ' color **mode** is 300 by 300 dpi. Apple's printers are faster than the HP and offer better color...

26/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01690166 SUPPLIER NUMBER: 15560951 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New uses for parallel ports. (Integration Connections)(includes related article on easing CPU load via parallel port modems) (Column)
Kennedy, Randall C.
Windows Sources, v2, n8, p197(2)
August, 1994
DOCUMENT TYPE: Column ISSN: 1065-9641 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1162 LINE COUNT: 00088

... bit port that has graced most systems since the early eighties and the more modern, 8-bit **bidirectional** port. The major difference is the number of bits that each type can receive from a communications...

...a time. With either type of parallel port, you'll see an immediate performance boost over traditional, **single - bit serial** ports.
If parallel ports are so much more efficient, why did it take so long for the...

26/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01687183 SUPPLIER NUMBER: 15510531 (USE FORMAT 7 OR 9 FOR FULL TEXT)
NSA bolsters SuperScan Elite 21-inch monitor. (NSA Hitachi SuperScan Elite 21) (Brief Article)
Bernard, Viki

PC Week, v11, n23, p25(1)
June 13, 1994
DOCUMENT TYPE: Brief Article ISSN: 0740-1604 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 205 LINE COUNT: 00016

... bandwidth to 160MHz.
Among several user controls are an RGB color control, an input terminal selector, a **mode** switch, brightness, contrast, **horizontal** /vertical position and size, an input terminal selector, and white-balance selection. Customers control these functions using a **serial** port that **links** the monitor and a nine-pin connector on the computer. Software bundled with the monitor allows users...

26/3,K/7 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01685070 SUPPLIER NUMBER: 15402962 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DeskJet 560C: HP's spectacular spectrums. (color ink jet printer) (includes related article on affordability of printer) (New! Hardware) (Hardware Review) (Evaluation)
Carlson, Kyla K.
PC-Computing, v7, n7, p70(1)
July, 1994
DOCUMENT TYPE: Evaluation ISSN: 0899-1847 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 791 LINE COUNT: 00059

... per-inch black and white; 300-dpi color.
Speed: 2 pages per minute (ppm) for black in **normal mode** ; 4 minutes per page (**mpp**) in **normal** color **mode** ; 7 **mpp** in presentation color mode.
Ink Cartridge Costs: $31.95 for black; $34.95 for color.
Ink Cartridge...

26/3,K/8 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01681143 SUPPLIER NUMBER: 15358612 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Color printing gets smarter hues. (HP DeskJet 560C ink-jet printer) (Hardware Review) (Evaluation)
O'Malley, Christopher
Computer Shopper, v14, n6, p355(1)
June, 1994
DOCUMENT TYPE: Evaluation ISSN: 0886-0556 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 930 LINE COUNT: 00069

... pace of the pages. Black print speed in Windows is rated at 2 pages per minute in **normal mode** and 3 ppm in fast mode. The best-quality presentation mode, used for gray-scale images, takes...

...expect, color takes a bit longer. Color print speed in Windows is measured in minutes per page (**mpp**): 7 **mpp** in presentation **mode** , 4 **mpp** in **normal mode** , and 3 **mpp** in fast mode. We found those ratings to be pretty accurate, though they vary with the software...

26/3,K/9 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01607585 SUPPLIER NUMBER: 14010319 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The office color printer. (HP introduces DeskJet 1200C/PS, a fast color inkjet printer) (New on the Menu) (Product Announcement)
Ito, Russell
MacUser, v9, n8, p40(1)
August, 1993
DOCUMENT TYPE: Product Announcement ISSN: 0884-0997 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 347 LINE COUNT: 00025

... megabytes of RAM. The result is a monochrome-text speed of 6 ppm (pages per minute) in **normal mode** (7 ppm in fast mode) and a color-graphics speed of 2 minutes per page (**mpp**), more than 1 ppm in fast mode.
To keep the 1200C/PS's output as sharp and...

26/3,K/10 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01602653 SUPPLIER NUMBER: 13972761 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New HP color laser printers. (HP Deskjet 1200C, 1200C/PS) (Product Announcement)
Rohrbough, Linda
Newsbytes, NEW05240028
May 24, 1993
DOCUMENT TYPE: Product Announcement LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 729 LINE COUNT: 00054

... Adobe's latest version of its page description language, Postscript Level 2.
The printers offer three print **modes** : **normal** , high quality, and fast. **Normal** is the default **mode** which the printer uses if no mode has been selected and HP says the majority of printing will be done in this **mode** . **Normal mode** offers 300 by 300 dpi text at 6 ppm and three-pass color graphics at 2 minutes per page (**mpp**).
High quality mode is slower, but offers better print quality. In this mode users can get 600...

26/3,K/11 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01544429 SUPPLIER NUMBER: 12912964 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mailing lists are a snap to print with MLPRINT. (Utilities)(includes related articles on obtaining utilities by modem, command reference card, updates to earlier utilities) (Column)
Munro, Jay
PC Magazine, v11, n21, p405(8)
Dec 8, 1992
DOCUMENT TYPE: Column ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4785 LINE COUNT: 00349

... not being used.
Printer Port: MLPRINT can print to LPT1 or LPT2. If your laser printer is **connected** to the **serial** port, use the DOS MODE command to redirect. The **normal** **MODE** command for redirecting LPT1 to COM1 is this:
MODE COM1:9600,N,8,1,P
MODE LPT1...

26/3,K/12 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01511970 SUPPLIER NUMBER: 12203805 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Empire helps PowerBook users accessorize. (Empire Engineering to introduce Second Serial Port Card, DC Power Adapter, AC pocket adapter for PowerBook portable computers) (brief article) (Product Announcement)
Cohen, Raines
MacWEEK, v6, n17, p9(1)
April 27, 1992
DOCUMENT TYPE: Product Announcement ISSN: 0892-8118 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 245 LINE COUNT: 00018

... 100s and gives users a second mini-DIN 8 RS-422 serial port, using the connector space **normally** reserved for a **modem** card. As a result, users can **connect** both a **serial** device and AppleTalk networks simultaneously.
>DC Power Adapter. The $99 device, due next month, fits into an...

26/3,K/13 (Item 13 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01500710 SUPPLIER NUMBER: 11972273 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Dialing for data. (Apple's AppleTalk Remote Access communications software package) (Bridges: Operating Systems) (includes a related article on dial-in servers with multiple serial **ports for** connection **to** modems **) (Column)**
Somogyi, Stephan
MacUser, v8, n4, p187(6)
April, 1992
DOCUMENT TYPE: Column ISSN: 0884-0997 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2413 LINE COUNT: 00179

...**Access communications software package) (Bridges: Operating Systems) (includes a related article on dial-in servers with multiple** serial **ports for** connection **to** modems **) (Column)**

26/3,K/14 (Item 14 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01440593 SUPPLIER NUMBER: 11004752 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bitwise: 386SX/16 Notebook; Micro Telesis: NBA386SX; National Micro Systems 386SX/16 Notebook. (Hardware Review) (one of 18 evaluations of 27 portable computers in '386SX Laptops: Desktop Power: Notebook Size') (evaluation)

O'Brien, Bill
PC Magazine, v10, n14, p136
August, 1991
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1234 LINE COUNT: 00093

... 3- by 6.8-inch triple-supertwist VGA LCD screen with 16 shades of gray in either **normal** or inverse screen **mode** , one parallel and two **serial** ports, **connectors** for an external monitor and a floppy disk drive, and DOS 3.3. There is no internal...

26/3,K/15 (Item 15 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01345253 SUPPLIER NUMBER: 08016960 (USE FORMAT 7 OR 9 FOR FULL TEXT)
HP printer cartridge brings PostScript to the LaserJet Series IID--fast. (Hewlett-Packard) (Hardware Review) (evaluation)
Mendelson, Edward
PC Magazine, v9, n2, p36(1)
Jan 30, 1990
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 526 LINE COUNT: 00040

... of the printer's ROM that governs the PostScript cartridge is different from the part that controls **normal** HP **mode** . With the PostScript cartridge plugged in, you will need to reconfigure the IID as a parallel printer, because the PostScript part of the printer's EPROM still thinks you're using the **serial connection** .
Until PC Labs made some slight changes in the way we downloaded the benchmark test files to...

26/3,K/16 (Item 16 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01204643 SUPPLIER NUMBER: 05042723 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Megabit dynamic RAMs target system solutions.
Bursky, David
Electronic Design, v35, p35(3)
July 9, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1481 LINE COUNT: 00109

... can be simultaneously read and fed into an on-chip exclusive-OR gate. The gate delivers a **single - bit** output to show when all bits match the desired value. If errors are found, the RAM can be switched back into its **normal mode** and every suspect bit location tested.
IBM's 4-Mbit design actually packs four independent 1-Mbit...

26/3,K/17 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2002 The Gale group. All rts. reserv.

04135961 SUPPLIER NUMBER: 16200390 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The right connections. (includes related articles on best buys,

installation, V.34 standard, checklist for buyers, online services and modems for portable computers) (Hardware Review) (high-speed fax modems) (Evaluation)
Angus, Jeffrey Gordon
PC World, v12, n9, p190(11)
Sept, 1994
DOCUMENT TYPE: Evaluation ISSN: 0737-8939 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6696 LINE COUNT: 00504

... have to be rebooted.
-- Either use an internal fax-modem or make sure your external model is **connected** through a **serial** port that uses a 16550 UART. About 50 percent of even the high-speed 486DX and Pentium...

...use the lower-end 8250 UART, which will almost certainly fail with a 28.8-kbps fax- **modem** working at its **normal** speed. You can buy a serial port that's equipped with a 16550.
To see which UARTs...

26/3,K/18 (Item 2 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2002 The Gale group. All rts. reserv.

02740631 SUPPLIER NUMBER: 04038512 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Parallel processing: fact or fancy? Parallel architectures are sprouting everywhere - but no everyone who claims to have one really does.
Serlin, Omri
Datamation, v31, p93(7)
Dec 1, 1985
CODEN: DTMNA LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4735 LINE COUNT: 00388

... node features an 8MHZ 286 MPU and a matching 287 numeric coprocessor. Internode communications are over 10Mbps **bidirectional bit - serial links** , controlled at each node by 82586 Ethernet chips. Intel testing shows each node is capable of about...

26/3,K/19 (Item 3 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2002 The Gale group. All rts. reserv.

02448221 SUPPLIER NUMBER: 02948632 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Businesspak+: getting down to business with the model 100. (evaluation)
Hart, Glenn A.
Creative Computing, v9, p79(3)
Oct, 1983
DOCUMENT TYPE: evaluation ISSN: 0097-8140 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 2689 LINE COUNT: 00202

... invoked the user is asked to select a text file which has been previously prepared using the **normal Model** 100 editor. A choice of Telex or ECOM is requested. The program asks for the Telex number (or name and address for an ECOM) of the recipient. A **pe** -stored default number can be selected if desired. The program then dials the local Action Telex office...

26/3,K/20 (Item 1 from file: 75)
DIALOG(R)File 75:TGG Management Contents(R)
(c) 2002 The Gale Group. All rts. reserv.

00164635 SUPPLIER NUMBER: 14536141 (USE FORMAT 7 FOR FULL TEXT)
Inferring market structure with aggregate data: a latent segment logit approach. (includes appendices)
Zenor, Michael J.; Srivastava, Rajendra K.
Journal of Marketing Research, v30, n3, p369(11)
August, 1993
ISSN: 0022-2437 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5775 LINE COUNT: 00505

... first question was investigated by comparing the likelihood of household purchase histories based on the homogeneous SB& **PE** model with each of the five segments of the LSL model. Figure 2 provides a plot of...

...LSL segment (the one with brand shares most similar to household level choice shares) over the SB& **PE** **model** . The **horizontal** axis in Figure 2 is that of McFadden (1974) |R.sup.2
(see Appendix B) relative to...

26/3,K/21 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

02462578 Supplier Number: 44927613 (USE FORMAT 7 FOR FULLTEXT)
Microsoft Mouse Software Upgraded 08/17/94
Newsbytes, pN/A
August 17, 1994
Language: English Record Type: Fulltext
Document Type: Newswire; General Trade
Word Count: 365

... scroll diagonally through spreadsheets with the mouse; the ability to lock the cursor into a horizontal or **vertical** movement only **mode** ; and sets of cursor animations that let the user turn the pointer into shapes like sailboats or...

...the bus version with its expansion card. A combination pack that comes with both PS/2 and **serial** **connectors** is also expected to sell for just under $90. The Intellipoint software is also available with Microsoft...

26/3,K/22 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

02090807 Supplier Number: 43857171 (USE FORMAT 7 FOR FULLTEXT)
New HP Color Laser Printers 05/24/93
Newsbytes, pN/A
May 24, 1993
Language: English Record Type: Fulltext
Document Type: Newswire; General Trade
Word Count: 695

... Adobe's latest version of its page description language, Postscript Level 2.
The printers offer three print **modes** : **normal** , high quality, and fast. **Normal** is the default **mode** which the printer uses if no mode has

been selected and HP says the majority of printing will be done in this **mode** . **Normal mode** offers 300 by 300 dpi text at 6 ppm and three-pass color graphics at 2 minutes per page (**mpp**).

High quality mode is slower, but offers better print quality. In this mode users can get 600...

26/3,K/23 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2002 The Gale Group. All rts. reserv.

01914182 Supplier Number: 43343862 (USE FORMAT 7 FOR FULLTEXT)
CROCKER INVESTMENTS OFFERS SOFTWARE DESIGNED FOR INVESTORS
PC Business Products, v4, n10, pN/A
Oct, 1992
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 535

... closing price and total volume, for the equity that you wish to chart. Set the price scale **vertically** and the volume scale **horizontally** . Now find the SINGLE point on the chart that correctly represents BOTH the price and the volume...

...SINGLE point on the chart that corresponds to BOTH the new price and the new volume. Finally, **connect** the two **successive** price-volume points with a **straight line** and use an arrowhead to indicate the time sequence between the two points. By repeating this procedure...

26/3,K/24 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

08286354 Supplier Number: 64690196 (USE FORMAT 7 FOR FULLTEXT)
Option Pricing: How Flexible Should the SPD Be?(Statistical Data Included)
LI, FENG
Journal of Derivatives, v7, n4, p49
Summer, 2000
Language: English Record Type: Fulltext
Article Type: Statistical Data Included
Document Type: Magazine/Journal; Academic Trade
Word Count: 8636

... 879)

% of Times (H.sub.0) Rejected	18.8	79.9	97.1

	Variable-Kurtosis		Fixed-Kurtosis	
Normal				
Model Category	T	**PE**		
LP BS				
Average Likelihood Ratio	147.926	146.184	169.934	197.477
	(10.597)		(10.597...	
...0.012 0.028				
Max	4.579	4.009	4.669	16.686

	Variable-Kurtosis		Fixed-Kurtosis	**Normal**
Model	T	**PE**	LP	BS
Mean	0.412	0.411	0.462	0.587

Standard Deviation 0.355 0.357...

...0.959
% of times (H.sub.0) Rejected 26.9 40.9
Model Category Variable-Kurtosis Fixed-**Normal**

Kurtosis
Nested **Models** GT T **PE**
LP BS

Average Z-statistic 5.541 5.663 5.541 7.115 8.047
% of times...

26/3,K/25 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

06107140 Supplier Number: 53689147 (USE FORMAT 7 FOR FULLTEXT)
Speeds, Duty Cycles Rise as Vendors Target the Small Office/Home Office Segment With New Printers -- Epson, HP Aim Color Inkjets at Businesses.(HP 2500Cse and Epson's Stylus Color 900 printers)(Product Announcement)
Koenig, Steve
Computer Retail Week, p13(1)
Feb 1, 1999
Language: English Record Type: Fulltext
Article Type: Product Announcement
Document Type: Magazine/Journal; Trade
Word Count: 323

... images, presentations, or graphics," he said.
The 900's print speed is around 10ppm for text in " **normal** " **mode** . Color pages, depending on coverage, can print at speeds close to 8ppm. To handle the demands of...

...900's duty cycle to 5,000 pages per month. The 900 includes standard interfaces for parallel, **serial** and USB **connections** .
HP's latest "workgroup" color inkjet, the 2500Cse, shipped in December.
At a $1,249 ESP, the...

26/3,K/26 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

04919734 Supplier Number: 47232435 (USE FORMAT 7 FOR FULLTEXT)
Stallion Technologies announces a networking industry first; New standalone remote access server extends NT-RAS for remote Microsoft NT users, offers cost-effective, integrated solution.
Business Wire, p03241039
March 24, 1997
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 673

... that networked serial ports are transparent to the application and allow all NT-based applications to operate **normally** over the **modem link** , with potential **serial** port performance speeds of 230Kbps.
"NERP is an unusual development in the networking industry, which

seems to...

26/3,K/27 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

04758769 Supplier Number: 47002842 (USE FORMAT 7 FOR FULLTEXT)
Prism reconfigures data warehouses
UNIX News, p32
Jan, 1997
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 155

... builds and maintains large-scale warehouses or operational data stores serving large numbers of users. This systems **normally** scales from a **moderate** NT server up to an **MPP** system; and finally, The PrismScaleable Conversion, which provides data conversion capabilities for migrating data across different application...

26/3,K/28 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

04657365 Supplier Number: 46852887 (USE FORMAT 7 FOR FULLTEXT)
VERSATILE NEW SUMMAGRAPHICS INKJET PLOTTERS OFFER FAST, UNATTENDED PLOTTING AND COLOR CAPABILITY AT LOW COST
News Release, pN/A
Nov 1, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 854

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...of $195 from the manufacturer. Performance and Productivity SummaCAD models provide a choice of four monochrome plot **modes** --draft, **normal** , enhanced and high-resolution monochrome--with selection depending on the desired output quality and plotting speed. In...

...Autodesk Device Interface) AutoCAD-optimized drivers, vector and raster data drivers for Microsoft Windows, and parallel and **serial** interfaces. For **connection** to a local area network, an external Ethernet interface supporting TCP/IP, Novell and EtherTalk is available...

26/3,K/29 (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

03897632 Supplier Number: 45614378 (USE FORMAT 7 FOR FULLTEXT)
Lunatic fringe' eyes fresh ideas
Electronic Engineering Times, p67
June 19, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1831

... of processor and memory with more-efficient use of DRAM-information

access. In the standard DRAM readout **mode** , an entire **row** of bits needs to be accessed to read a **single bit** . The 'processor-in-memory' architecture, by contrast, directly loads rows into the 16-bit registers of the...

26/3,K/30 (Item 7 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

02461183 Supplier Number: 43245066 (USE FORMAT 7 FOR FULLTEXT)
Zilog respins Z80 chip
Electronic Engineering Times, p56
August 24, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 497

... the pin count. Zilog anticipates selling this part into internal and external modems. But while an external **modem normally** interfaces to the serial port on the back of a PC, an internal modem must talk directly ...

...can function normally, meaning it talks to a serial port, or it can mimic a standard 16550 **serial** port, **connecting** directly to an AT or XT bus.
The part also has some new electrical features to meet...

26/3,K/31 (Item 8 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2002 The Gale Group. All rts. reserv.

01059683 Supplier Number: 41174279
APM SALES & MARKETING CORP., 90 13th Avenue, Ronkonkoma, New York., now makes available a new compact horizontal wrapper, Model Speedy 1, with speeds up to 100
News Release, p1
Feb 15, 1990
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Trade

ABSTRACT:
APM SALES & MARKETING CORP., 90 13th Avenue, Ronkonkoma, New York., now makes available a new compact **horizontal** wrapper, **Model** Speedy 1, with speeds up to 100 packages per minute. Unit is designed to accept products in...

...19" and height up to 3 1/2". Unit is designed to seal OPP, Cellophane, Polycel, Zeelon, **PE** /Paper Foil/Polyethylene. It uses readily available roll-stock film to produce a package with a fin...

26/3,K/32 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)
(c) 1999 The Gale Group. All rts. reserv.

00410351
One-operation blown-film coextrusion permits economical production of combination films through multilayered production at favorable costs due to the optimization of essential parts of the extrusion line.

Modern Plastics February, 1978 p. 56-581

...non-rotating die. Wide films from materials processed at below 220 C can be produced in polyethylene (**PE**) combination lines using **modern** -design **horizontal** extruders. Universal lines to process polyamides (PA) have been developed to meet the requirements of packaging films...

Search report

Set	Items	Description
S1	21381	MASSIVELY()PARALLEL()PROCESSOR? OR MPP OR PLURALITY()PROCESSING()ELEMENT? OR PPE OR PE OR PROCESSOR()(ARRAY? OR ARRANGEMENT? OR ORDER OR FORMATION)
S2	6366	(SERIAL? OR CONSECUTIVE? OR SUCCESSIVE? OR SEQUENTIAL?)(2N)(CONNECT? OR LINK?) OR SINGLE()BIT
S3	4995	MODE? (3N) (VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?)
S4	7646	MODE? (3N) (HORIZONTAL? OR ROW OR NORMAL?)
S5	607	MODE? (3N) (BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE)
S6	139	VERTICAL()(MEMORY OR STORE? OR STORAGE OR ROM)
S7	340110	VERTICAL? OR UPRIGHT? OR BIT()SERIAL? OR COLUMN?
S8	594470	HORIZONTAL? OR ROW OR NORMAL?
S9	46247	BIDIRECTION? OR BI()DIRECTION? OR OPPOSITE()DIRECTION? OR PERPENDICULAR? OR STRAIGHT()LINE
S10	0	S1 (S) S2 (S) S3 (S) S4 (S) S5
S11	5	S1 (S) S2
S12	27695	S1 OR S2
S13	0	S12 (S) S3 (S) S4 (S) S5
S14	4	S12 (S) S3
S15	24	S12 (S) S4
S16	0	S15 (S) S5
S17	1	S12 (S) S5
S18	0	S12 (S) S6
S19	462	S12 (S) S7
S20	84	S19 (S) S8
S21	6	S20 (S) S9
S22	52	S1 AND S2
S23	0	S22 (S) S3
S24	1	S22 (S) S4
S25	0	S22 (S) S5
S26	0	S22 (S) S6
S27	2	S22 (S) S7
S28	2	S22 (S) S8
S29	3	S22 (S) S9
S30	39	S14 OR S15 OR S17 OR S21 OR S24 OR S27 OR S28 OR S29
S31	32	S30 NOT PY>2000
S32	30	S31 NOT PD>20000831
S33	30	RD (unique items)

File 15:ABI/Inform(R) 1971-2002/Jul 30
(c) 2002 ProQuest Info&Learning
File 647:CMP Computer Fulltext 1988-2002/Jul W4
(c) 2002 CMP Media, LLC
File 674:Computer News Fulltext 1989-2002/Jul W3
(c) 2002 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2002/Jul 29
(c) 2002 The Dialog Corp.
File 98:General Sci Abs/Full-Text 1984-2002/Jun
(c) 2002 The HW Wilson Co.
File 624:McGraw-Hill Publications 1985-2002/Jul 30
(c) 2002 McGraw-Hill Co. Inc
File 369:New Scientist 1994-2002/Jul W1
(c) 2002 Reed Business Information Ltd.
File 484:Periodical Abs Plustext 1986-2002/Jul W3
(c) 2002 ProQuest
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2002/Jul 30
(c) 2002 PR Newswire Association Inc
File 141:Readers Guide 1983-2002/Jun

(c) 2002 The HW Wilson Co
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 553:Wilson Bus. Abs. FullText 1982-2002/May
(c) 2002 The HW Wilson Co

33/3,K/1 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

02244797 86923926
Sensor gateway to fieldbuses
Derek Paul Lane
Sensor Review v17n3 PP: 211-216 1997
ISSN: 0260-2288 JRNL CODE: SEN
WORD COUNT: 3557

...TEXT: communication protocol (invented by Stegmann) on RS422 to communicate between the encoder and input module.

High-speed **bi - directional** counters ensuring pulses of up to 100KHz at 24V DC are captured. These have two input signals, one for the up pulse and one for down pulse. This would allow position tracking of a **single bit** , or entry/exit values giving contents inside, such as a car park. The position register can be...

33/3,K/2 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

02036543 55345175
Advanced transportation controller standards overview
Anonymous
Institute of Transportation Engineers. ITE Journal v70n6 PP: 26-29 Jun 2000
ISSN: 0162-8178 JRNL CODE: TE
WORD COUNT: 3505

...TEXT: impact on the software investment.

ACKNOWLEDGMENTS

The ATC Steering Committee acknowledges the work of Paul R Olson, **PE** ., FHWA Western Resource Center, who lead the effort to author this **column** , and the leadership of Raj Ghanian, FHWA Research and Development, who championed the ATC initiative from its...

33/3,K/3 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

01915826 05-66818
Conversion of signal-timing plans into traffic-controllers parameters
Khatib, Zaher K; Coffelt, Paul B
Institute of Transportation Engineers. ITE Journal v69n8 PP: 36-40 Aug 1999
ISSN: 0162-8178 JRNL CODE: TE
WORD COUNT: 3123

...TEXT: by one of two methods.

With the simplest method, interface software is installed, which enables a PC **serial connection** to the controller in the field and allows data transfer on site. The second method is to make the **serial connection** with modems, so engineers and technicians can dial into controllers and

change timings from remote locations such as a traffic-control center. Interface programs are **normally** designed for userfriendly data exchange and programming of complete controller functions, including splits.

During signal-timing design...

33/3,K/4 (Item 4 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

01899447 05-50439
NEC debuts new 50-inch Plasma
Simons, Tad
Presentations v13n9 PP: 20 Sep 1999
ISSN: 1072-7531 JRNL CODE: PRS
WORD COUNT: 225

...TEXT: more realistic-looking picture.

Among the other features included with the 5000W are an RS-232-compatible **serial connection** and an intelligent image-- scaling system that enables the monitor to display conventional computer graphics and video with a 4:3 aspect ratio, as well as 16:9 images in four different **modes** : **normal** , full, stadium and zoom. The unit also comes with a hand-held remote and includes a built...

33/3,K/5 (Item 5 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

01235595 98-84990
Axil's S/420 HyperSPARC server
Barker, Ralph
UNIX Review v14n8 PP: 53-58 Jul 1996
ISSN: 0742-3136 JRNL CODE: UXR
WORD COUNT: 2354

...TEXT: controller in the subsystem, along with associated configuration utilities. Earlier models of the S/420 provide a **serial** communication **link** between the main chassis and the RAID subsystem. To configure the RAID subsystem, the installer uses the...

... RAID level 5 is the desired configuration, the installed disks can be formatted and mounted in the **normal** manner. Newer **models** of the S/420 provide a utility that configures the subsystem directly via the SCSI bus.

Documentation...

33/3,K/6 (Item 6 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

01050445 96-99838
What's new
Warner, Paul D
CPA Journal v65n6 PP: 64-65 Jun 1995
ISSN: 0732-8435 JRNL CODE: CPA
WORD COUNT: 994

...TEXT: well as mixed computing environments.

Operating Modes

The printers have three modes of print quality and speed:

* **Normal mode** (the default **mode** and the mode HP believes will account for more than 70% of the printer's use) produces...

... x 300 dpi text at 6 ppm and three-pass color graphics at 2 minutes per page (**mpp**).

*High-quality mode which provides superior print quality for text and color--producing 600 x 300 dpi...

33/3,K/7 (Item 7 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

00940060 95-89452
Designing reliability into solid-state disk emulators
Tuma, Wade
Computer Technology Review v14n10 PP: 52 Oct 1994
ISSN: 0278-9647 JRNL CODE: CTN
WORD COUNT: 1066

...TEXT: of errors that are most predominant in SSDs will rarely be corrected by this error recovery technique.

ROW MODE ERROR CORRECTION

Row mode error correction technology was originally developed to error-correct main memory in CPUs. This type of error...

...bits of additional data must be appended to each row to allow double-bit error detection and **single bit** error correction. Thus this type of error detection correction system can repair one error in every 64...

33/3,K/8 (Item 8 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

00652614 93-01835
Integrators Write Rx for Lazy CPUs: Communications Servers Put Them to Work
Trowbridge, Dave
Computer Technology Review v12n13 PP: 1, 11 Nov 1992
ISSN: 0278-9647 JRNL CODE: CTN
WORD COUNT: 1736

...TEXT: capability thus leaves many UNIX users in the lurch when they seek to connect printers, terminals, or **modems** to these systems. **Normally** , multiport serial I/O boards are the answer, but they require an expansion slot. What's a...

... and not yet common. The first, long familiar in the DEC world, is the terminal server, which **connects serial** devices to an Ethernet and handles all the protocol processing needed to connect terminals, printers, and modems...

33/3,K/9 (Item 9 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

00631028 92-45968
Handheld Computing
O'Brien, Terrence V.
Marketing Research: A Magazine of Management & Applications v4n2 PP: 34-36 Jun 1992
ISSN: 1040-8460 JRNL CODE: MRE
WORD COUNT: 2098

...TEXT: pressed, the next key pressed is shifted, such as upper case. The shift key works in the **normal** hold-it-down **mode** , too.) **Connects** to standard **serial** devices, such as a modem, printer, or fax modem. With converter ($99 at Radio Shack), a parallel...

33/3,K/10 (Item 10 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2002 ProQuest Info&Learning. All rts. reserv.

00607067 92-22170
Factors Affecting Price Earnings Ratios and Market Values of Japanese Firms
Constand, Richard L.; Freitas, Lewis P.; Sullivan, Michael J.
Financial Management v20n4 PP: 68-79 Winter 1991
ISSN: 0046-3892 JRNL CODE: FMG
WORD COUNT: 7566

...TEXT: Our results suggest that variables such as risk, earnings and dividend growth, and dividend payout, that are **normally** associated with textbook **models** of **PE** ratio, are also significantly related to changes in both **PE** ratio and market value changes in Japanese firms. Furthermore, the rise in **PE** ratios and market values are not a consequence of a decrease in the required rate of return...

... industrialized nations. The results associated with the change in special reserves support an earnings-based influence on **PE** ratios and market values.

We summarize our results as follows. The primary factors behind the dramatic increase...

33/3,K/11 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

01183737 CMP ACCESSION NUMBER: CRW19990201S0021
Speeds, Duty Cycles Rise as Vendors Target the Small Office/ Home Office Segment With New Printers - Epson, HP Aim Color Inkjets at Businesses
Steve Koenig
COMPUTER RETAIL WEEK, 1999, n 233, PG13
PUBLICATION DATE: 990201
JOURNAL CODE: CRW LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Business Solutions
WORD COUNT: 325

... images, presentations, or graphics," he said.

The 900's print speed is around 10ppm for text in " **normal** " **mode** . Color pages, depending on coverage, can print at speeds close to 8ppm. To handle the demands of...

...900's duty cycle to 5,000 pages per month. The 900 includes standard interfaces for parallel, **serial** and USB **connections** .

HP's latest "workgroup" color inkjet, the 2500Cse, shipped in December.

At a $1,249 ESP, the...

33/3,K/12 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

01056557 CMP ACCESSION NUMBER: EET1995061950055
Conference explores 'silicon publishing,' other leading-edge notions - 'Lunatic fringe' eyes fresh ideas (CROSSTALK)
Chappell Brown
ELECTRONIC ENGINEERING TIMES, 1995, n 853, PG67
PUBLICATION DATE: 950619
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: TECHNOLOGY
WORD COUNT: 1820

... of processor and memory with more-efficient use of DRAM-information access. In the standard DRAM readout **mode** , an entire **row** of bits needs to be accessed to read a **single bit** . The "processor-in-memory" architecture, by contrast, directly loads rows into the 16-bit registers of the...

33/3,K/13 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

00632876 CMP ACCESSION NUMBER: EET1989112050989
Modules for embedded PCs
KATHY ROGERS
ELECTRONIC ENGINEERING TIMES, 1989, n 565, 46
PUBLICATION DATE: 891120
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: DES
WORD COUNT: 409

... I/O ports. It consists of two ports. One is bidirectional parallel port; the other is a **serial link** that can be configured an an RS-232-C, RS-422 and RS-485 link. The parallel port can be used as a Centronics-compatible printer port or for general-purpose **bidirectional** I/O.
MM/ **Modem** features all the circuitry of an industry-standard 2,400-baud Hayes-compatible modem. It also includes...

33/3,K/14 (Item 4 from file: 647)

DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

00576594 CMP ACCESSION NUMBER: UNX199001225S4435
SOFTWARE Product: Microshop IV Version 2.4, job shop manufacturing software.... (Products Briefs)
UNIX TODAY , 1990, n 037, 35
PUBLICATION DATE: 900122
JOURNAL CODE: UNX LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: PRODUCTS
WORD COUNT: 1653

... controller brings multiple users and timesharing to SPARCstation by allowing up to 8 simultaneous asynchronous or synchronous **serial connections** per expansion board. Each port features full modem control and a baud rate from 300 to 38...

...software driver, allows connection to any Centronics-compatible printer or can be used as a general-purpose **bidirectional** parallel port for interfacing to any device using standard signal levels.
Circle Reader Service No. 209
Product...

33/3,K/15 (Item 5 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

00544691 CMP ACCESSION NUMBER: WIN19931101S3045
Carbon Copy 2.0 - Easy File Transfer
Rick Vizachero
WINDOWS MAGAZINE, 1993, n 411 , 118
PUBLICATION DATE: 931101
JOURNAL CODE: WIN LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: First Impressions
WORD COUNT: 712

... drop, to move files across the wires between computers.
Carbon Copy lets you control computers across LAN **connections** , directly wired **serial connections** and communications servers as well as the **normal modem** link. The manual selection of 134 modems is passable, but a program that auto-recognizes the modem...

33/3,K/16 (Item 6 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2002 CMP Media, LLC. All rts. reserv.

00509766 CMP ACCESSION NUMBER: EET19920824S2634
Zilog respins Z80 chip
RON WILSON
ELECTRONIC ENGINEERING TIMES, 1992, n 707, 56
PUBLICATION DATE: 920824
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design - Solid State
WORD COUNT: 502

... the pin count. Zilog anticipates selling this part into internal

and external modems. But while an external **modem** **normally** interfaces to the serial port on the back of a PC, an internal modem must talk directly...

...can function normally, meaning it talks to a serial port, or it can mimic a standard 16550 **serial** port, **connecting** directly to an AT or XT bus.
The part also has some new electrical features to meet...

33/3,K/17 (Item 1 from file: 696)
DIALOG(R)File 696:DIALOG Telecom. Newsletters
(c) 2002 The Dialog Corp. All rts. reserv.

00728337
Broadband Bulletin
CableFAX
May 31, 2000 VOL: 11 ISSUE: 106 DOCUMENT TYPE: NEWSLETTER
PUBLISHER: PHILLIPS BUSINESS INFORMATION
LANGUAGE: ENGLISH WORD COUNT: 480 RECORD TYPE: FULLTEXT

(c) PHILLIPS PUBLISHING INTERNATIONAL All Rts. Reserv.

TEXT:
...NetGame and GVC, the last of which was certified as "plug-and-play" due to its
universal **serial** bus **connector** that dispenses with the need to have an Ethernet
card installed on the computer. 3Com [COMS] had...

...in its 3Q over the next two quarters now
that Motorola [MOT] has increased its supply of **modems** to " **normal** ."

Int'l
UPC's [UPCOY] Chello broadband 'Net access unit delayed its $717mln (773mln euros) IPO until...

...Supply

Good news for Shaw [SJR] from Motorola [MOT] as Motorola has restored its supply of cable **modems** to **normal** , effectively May 30, and this has allowed Shaw
to renew its marketing campaigns. Motoroal has also provide...

33/3,K/18 (Item 1 from file: 98)
DIALOG(R)File 98:General Sci Abs/Full-Text
(c) 2002 The HW Wilson Co. All rts. reserv.

04255643 H.W. WILSON RECORD NUMBER: BGSA00005643 (USE FORMAT 7 FOR FULLTEXT)
Meiotic chromosomes: integrating structure and function.
AUGMENTED TITLE: review
Zickler, D
Kleckner, N
Annual Review of Genetics v. 33 (1999) p. 603-754
SPECIAL FEATURES: bibl il ISSN: 0066-4197
LANGUAGE: English
COUNTRY OF PUBLICATION: United States
WORD COUNT: 73948

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... a surface, are helpful (in permitting the analysis of many more nuclei than can be analyzed by **serial** sections) to study a specific problem, e.g. synapsis or interlockings (e.g. 407, 465), recombination nodule...several mutants defective in SC formation, at a more or less reduced level compared to wild type. **Normal** numbers of meiotic chromosome pairing interactions, with concomitant full homolog coalignment, occur in hop1 and spo11-Y135F...frequent (52); both defects may be manifestations of aberrant pairing. These findings provide evidence that homolog pairing **normally** occurs in such a way that interlocking is avoided. Second, in certain images of nuclei containing interlockingsconcomitantly encircling one or more other chromosomes. By inference, such interlocks are **normally** avoided by early homolog colocalization. Third, interlockings can be induced by premeiotic colchicine treatment (502) or heat...

...to spend relatively more time in zygotene, which would give the same appearance as greater abundance with **normal** stage durations. Finally, the nuclei with several interlocks might remain blocked at zygotene and thus never be...a defined locus on the long arm of chromosome 5B). When this locus is present in its **normal** complement, with chiasma formation restricted to the homologous chromosomes, only bivalents are observed at metaphase I (152...in chromosomes that are mosaics of homologous and homeologous regions, in the presence of Ph1, crossovers occur **normally** in the homologous regions but not in the homeologous regions of the same chromosomes (299). Similarly, in...

...strand breaks (DSBs) occur equally on both chromosomes; nonetheless, the rate of formation of intragenic recombinants (which **normally** arise mostly via heteroduplex DNA) is reduced 40-fold as compared to the homologous control. Moreover, in...using a mitotic model system, suggests that the occasional intragenic recombinants that arise between homeologous sequences are **normally** resolved as "gene conversions" rather than crossovers and that mismatch repair components limit the extent of heteroduplex...

...few organisms SCs are reported to lack CEs. The green alga Ulva (591) and Chlamydomonas (882) show **normal** LEs and central region but no CE. All Meloidogyne (nematodes) species studied thus far (except M. microtyla) show **normal** AE/LEs but lack CEs and often also exhibit a narrow (30-40 instead of 100 nm...from the spo22 mutant of Coprinus cinereus: this mutant, defective in premeiotic DNA replication, forms nevertheless completely **normal** SCs (400). It further appears that LE/AE organization corresponds to chromatin loop organization (section below).

MORPHOLOGICAL...

...in several organisms and mainly take the form of swellings or thickenings of different lengths, on otherwise **normal** LEs (reviewed in 173, 289, 654). Unsynapsed AEs of the same species do not show deformities; abnormalities...PCs have, however, been observed only rarely. In the mosquito Culex pipiens oocytes, the transverse filaments, which **normally** span the central region, pass outside the SC, extend and attach to the LE of another bivalent...I, and are segregated through both meiotic divisions (534).

c. Multiple SCs can be seen associated to **normal** synapsed SCs at pachytene apparently without effect on meiosis or recombination as in Neurospora (52). In tomato...

...these types of effects may account for much of the variability observed

in what is otherwise apparently **normal** meiosis (discussed above).

MORPHOLOGIES

The detailed architecture, size, and shape of polycomplexes are highly variable between organisms...

...formation. In contrast, the dense elements of PCs show much more morphological variation as compared to the **normal** AE/LE structure on chromosomes: Sometimes their thickness is sufficient to account for the width expected when...

...the formation of extensive amounts of PCs (Form I and networks) in a strain that does not **normally** produce such structures (492). Third, when the length of the Zip1 protein is altered by increasing the...assemble independently of the AE components Hop1p and Red1p (492). Moreover, other proteins like Zip2p and Pch2p, **normally** located onto the AE and the nucleolus, respectively, are also located in PCs resulting from overexpression of...two chiasmata, the pairs of homolog arms in adjacent inter-chiasma intervals appear to lie in two **perpendicular** planes and, in addition, are bent or curved. This phenomenon, usually referred to as repulsion, but perhaps...

...close. Second, "there is a tendency for the chromosomes or chromosome parts to arrange themselves parallel or **perpendicular** to each other ... clearly seen during straightening of the arms in c-anaphase when, after separation, the chromatids tend to arrange themselves **perpendicular** .... Also, if a chromosome arm forms a loop the angle at the crossing is approximately 90[degree...

...436). Most recently, polymer models have been considered for this and other aspects of chromosome organization (311).

NORMAL SC IS SOMETIMES ABSENT

SCs are absent in three fungi, Schizosaccharomyces pombe (24, 377, 731), Ustilago maydis...

...recombination and premature segregation of sister chromatids at meiosis I (352), phenotypes also observed in mutants lacking **normal** AE/LEs in other organisms, including a rec8 mutant of budding yeast (267; see below).

ACHIASMATE MEIOSIS--WITH AND WITHOUT SC

Organisms that lack chiasmata at diplotene (Figure 9) can still exhibit **normal** SC as shown for achiasmate male Bolbe nigra (168) and Panorpa communis (528), in achiasmate female of Bombyx mori (404, 813), and Ephestia kuehniella (310, 504). In all four species, SCs form **normally** at early prophase but, instead of disappearing at diplotene as in the standard program, are retained until...

...is otherwise regular, the 4th chromosome rarely undergoes crossing over but shows regular SC confined to the **normal** prophase stages just as for other chromosomes (75, 198). Here, however, no stable connection between the homologs is present at metaphase I and backup mechanisms ensure **normal** disjunction (198). A case of meiosis without recombination has also been reported in Saccharomyces ludwigii (e.g...regions that would indicate an alteration in underlying organization. No differences are seen in sectioned material or **normally** spread material of tomato (though unique AE/LE morphology can be revealed by DNase I treatment plus...Correspondingly, whereas l DNA minichromosomes in yeast are nearly inert for recombination (425), human YACs exhibit substantially **normal** behavior for recombination and chromosome segregation (235, 448, 449, 730). Similarly, and

dramatically, when Xenopus sperm are...AE CAN BE SINGLE OR DOUBLE
The AE/LE, like the bulk chromatin of each sister pair, **normally** appears as a single morphological unit. In some situations, however, duality is directly observable; in addition, "splitting...

...an AE. In this mutant, homologous maternal and paternal chromatids still identify one another and form apparently **normal** SC (400).

Evidence for functional duality in **normal** chromosomes is also suggested by the finding that two SCs can share a single LE. In triploids ...

...two flanking central regions, yielding either a planar or a triangular array. Such observations imply that the **normal** LE, despite its unitary morphological appearance, can be functionally double with respect to its capacity to organize...

...chromatids coalign, SC forms only pairwise; no triple synapsis is observed. It was inferred that whereas a **normal** AE is functionally double and thus can join with two central regions, a unitary one-chromatid axis...

...observed singleness of LEs at zygotene, but discernible doubleness by early to mid-pachytene in the plane **perpendicular** to the SC (with coordinately denser and thicker appearance); then, at late pachytene, LEs become progressively more...

...at the leptotene/zygotene transition. In the spo76-1 mutant of Sordaria, AEs initially form in the **normal** unitary way but then split at the leptotene/zygotene transition (512, 783). Along mutant chromosomes at this ...

...reflects the response to a disruptive force that occurs at the leptotene/zygotene transition. This force would **normally** be channeled via Spo76 into some important step of chromosome morphogenesis; in spo76-1, by contrast, the...

...F1 hybrid of an interspecific cross: the X/Y chromosome pair exhibited either of two alternative morphologies: **normal** SCs and chromatin or failure of synapsis plus diffuse chromatin (763).

Reports of splitting along leptotene chromosomesSISTER CHROMATIDS ARE STACKED **VERTICALLY** AT THE EDGES OF THE SC RIBBON
Dresser & Moses (137) argued from early spreading studies that sister chromatid subaxes were parallel and lay in a plane **perpendicular** to the SC axis (see also 372) (Figure 10) in support of earlier studies. Ultrastructural analysis of...loops and spacers present in the same chromosome at the immediately preceding pachytene stage? Newt chromosomes exhibit **normal** pachytene and diffuse diplotene stages immediately prior to the lampbrush stage and then, subsequently, exhibit a modified... sections of rat, hamster (129, 327, 441), and mouse SCs (288) suggest that SCP1 molecules are oriented **perpendicularly** to the LEs with two fully extended molecules spanning the central region in a tail-to-tail...

...strains results in formation of numerous polycomplexes, as analyzed in a strain background where PCs do not **normally** occur (492).
The organization of Zip1 within pachytene chromosomes appears to be similar to that of SCP1...

...of Zip1--in Brief Zip1 protein is not strongly required for intersister relationships: AE morphogenesis is apparently **normal** (compare Figure 2a and Figure 14), and sisters usually segregate together at meiosis I, even

when homologs...
...where cell cycle arrest/delay is less severe, the total number of recombinational interactions appears to be **normal** , as assessed both genetically and physically, but the array of product types is severely affected (483, 491...the protein is overproduced or in a zip1 mutant where SC does not form (461), implying a (**normally** restrained) propensity for spreading. Double immunofluorescence staining with anti-Red1p and anti-Hop1p shows extensive colocalization; ...by FISH (25). A red1 mutant fails to assemble any discernible AE or SC structure and exhibits **normal** chromosome compaction. A hop1 mutant forms long fragments of AEs, but no SCs and is defective in...

...such arrest occurs if a red1, hop1, or mek1 mutation is present. This latter finding implies that **normal** chromosome structure is important if the cell is to monitor the progression of chromosome metabolism. This effect could be indirect, because **normal** chromosome structure is required for assembly of a **normal** interhomolog recombination complex (see below) or direct, because chromosome structure per se is involved in monitoring.
Yeast...422). Hop2 is thus suggested to play an important role during the first steps of recombination which **normally** , in some way, constrain SC formation to occur between homologs (282).
Rec8 Rec8, identified originally in S...
...of pachytene spermatocytes (8). Moreover, in the absence of this protein, spermatocyte meiosis arrests at pachytene, with **normal** SC formation (128), and without activation of CDC2 kinase activity (930), possibly as a consequence of the...including topoisomerase II (892). In mitotic cells, S-phase and formation of chromosome cores can proceed relatively **normally** in the absence of TopoII activity though not necessarily in the complete absence of TopoII protein (485...auxiliary features. An example might be yeast Pch2 protein, whose absence does not affect spore viability during **normal** meiosis but does affect checkpoint control and recombination in the specialized rDNA compartment (431).
Fifth, the recombination...

...which show both a decreased frequency of crossovers and a defect in interference (491). Thus, it is " **normal** " that most or all of the proteins involved in the recombination processes are located onto the chromosome...

...of mammalian spermatogenesis, unique changes occur that are thought to represent the beginning of a transition from **normal** histone arrays to protamines, via transition proteins, during packaging of chromosomes into sperm. A testis-specific H1...the role of Pch2 in meiotic prophase checkpoint arrest (431). The meiosis-specific axis component Hop1p, which **normally** localizes only to AE/LEs, is found in the nucleolus in both pch2 and sir2 mutants, in...

...exhibits defects in recombination and spore formation (89, 755). SC formation and chromosome compaction and decompaction appear **normal** , however. Mutations in one of two Bdf1 bromodomains confer only meiotic defects (...the presence of both is correlated with the formation of LNs in the female (74, 75). While **normal** SCs are observed in male and female Bombyx, LNs form in the chiasmate spermatocytes, but not in...mutants, mei-W68 (defective in the Drosophila homolog of yeast DSB transesterase Spo11) and mei-P22, exhibit **normal** SCs but no nodules, crossovers, or intragenic recombination (321, 322). The mei41 mutant homolog of cell cycle...

...to 8[percent] of wild type and crossover interference is abolished but intragenic recombination at rosy is **normal** or enhanced, with shorter conversion tracts than the control (83); both types of nodules are reduced to...some nuclei (27, 32, 33).

Mlh1 is implicated functionally in meiotic recombination. In mouse, mlh1 -/- spermatocytes show **normal** pachytene and diplotene but strongly reduced levels of chiasmata, leading to almost only univalent formation at metaphase I (27, 536) or, in another line, pachytene arrest (140). Mouse mlh1 -/- oocytes similarly exhibit **normal** synapsis but reduced chiasmata (27, 140). Such differences are common for yeast meiotic mutant phenotypes in different...

...5 has been implicated in intermediate or late steps of recombination: it is required for a qualitatively **normal** array of products (426, 697) and for crossover interference (423) but is not required for DSB formation or for a **normal** number of recombinational interactions. The msh4/5 phenotype is the same as that observed for zip1 and...type yeast meiosis; they may be too transient for detection or they may represent morphologies that are **normally** found within the context of the SC.

These considerations emphasize that recombination-related homolog juxtaposition reflects not...

...Patches of SC with an associated LN are routinely found where SC is discontinuous or absent, in **normal** meiosis at prophase (e.g. 53, 120, 480; reviewed in 6, 474, 519) or diplotene (see above...

...Their Components) and Recombination We are not aware of any mutant in any organism that has completely **normal** recombination but defective SC formation. This pattern would seem to imply that fully **normal** recombination cannot be uncoupled from SC formation. In yeast, SC polymeriozation occurs well after DSB formation (378 an SC central region component, appear to exhibit essentially **normal** total numbers of recombinational interactions (above). Thus, in this organism, SC formation and/or the presence of...

...mutant that make full-length AEs. In contrast, mutants that get as far as DSB formation (at **normal** levels, with or without resection) make at least some SC. But no mutant has thus far been found to be recombination defective and to give **normal** SCs. Moreover, the farther along the recombination pathway the mutant can proceed, the more SC is formed...

...opportunities for interdependence of meiotic recombination and SC formation.

Many mutants in organisms other than yeast exhibit **normal** SC but are defective in recombination (below); that is, SC formation can be uncoupled from recombination. No...

...the relationship between recombination and the SC.

SC Can Occur Without Crossing Over Situations in which apparently **normal** SC forms but crossing-over (manifested genetically or cytologically) is defective, reported recently for mlh1 mice (above...

...the notable exception of two-phase synapsis adjustments, to remain stable, in the absence of a fully **normal** recombination process, is a quite universal property.

In Some Organisms, **Normal** SC Formation Can be Uncoupled from Recombination Initiation In Drosophila and C. elegans, **normal** SC formation is observed in mutants lacking the respective SPO11 homologs (122, 321). This could mean that SC formation is **normally** independent of DSB formation, which would open the possibility that SC formation might precede initiation of recombination...

...Moreover, a recent yeast study demonstrates that gamma irradiation of a spo11 mutant at the time of **normal** DSB formation induces appearance of elongated Zip1 immunostaining structures (which are absent in unirradiated

mutant cells); these...

...the yeast genome by HO endonuclease cleavage during meiosis can provoke high levels of crossing over, with **normal** dependency on meiotic recombination functions known to act after DSB formation (e.g. MSH4/5; R Malkova...all imply that, irrespective of the extensive programming which guide DSB formation and SC formation during the **normal** meiotic program, reasonably robust meiosis can be achieved in the absence of such features. This conclusion is...
...elegans, where SC forms in the absence of recombination initiation. On the other hand, such organisms may **normally** exhibit exactly the same program as inferred for other cases and differ only with respect to the potency of secondary SC nucleation mechanisms, which can promote SC formation in a relatively **normal** time frame even when **normal** nucleation mechanisms are missing.

Crossover Control and the SC A correlation between crossover commitment and nucleation of...containing CEN3 plus surrounding sequences can, when inserted, act in cis to suppress meiotic recombination in a **normally** active region (273). This finding can be linked to the cohesins distribution by the finding that a...

...binding of cohesins in artificial chromosomes (D Koshland, personal communication). Second, in fission yeast, meiotic recombination is **normally** several-fold lower near centromeres than in arms (331); moreover, three genes, rec8, rec10, and rec11 specifically...rest of the genome (above; 445). Furthermore, rDNA recombination occurs by a different (RAD50-independent) pathway than **normal** meiotic recombination (185). Meiotic rDNA recombination, both between homologs and between sisters, is suppressed by the chromatin...

...to genetic perturbation. Finally, while recombination-less (achiasmate) meiosis might reflect any number of variations from the **normal** program, the chromosomes of such organisms could formally be considered whole genome compartments, with the absence of...

...512). An analogous defect is observed in mitotic cells, at prometaphase, although chromosome morphology at metaphase is **normal** . The meiotic spo76-1 defect results in a block to recombination, apparently at the DSB to dHJ transition. It is inferred that, for **normal** chromosomes, the leptotene/zygotene transition includes the transient imposition of a disruptive force, here referred to a "stress", whose effects are **normally** transduced into effects on the recombination process. The imposed stress could then be relieved in a specific...including crossovers. (d) Rad51 foci occur at non-matching positions along unsynapsed homologs (31), implying that DSBs **normally** do not occur at corresponding positions. (e) Axis-associated DSB formation could provide an opportunity for differentiating...These events would guided in some way by the underlying DNA. Also, recent work shows that proteins **normally** associated with the chromosome axes, e.g. SCP2, SMC1, SMC3, and possibly also SCP3, are found in...

...at post-pachytene stages (434, 841). This could suggest that axis-associated proteins "ooze" out of their **normal** locations along the crossover-associated DNA to form these structures. Ultimately, however, once recombinant axes have developed...expected to affect the recombination process via "coupling defects," causing either recombinational processes to be uncoupled from **normal** chromosomal or nuclear processes or, conversely, the recombination process to be blocked at an important barrier and...

...post-DSB recombination-related processes can still function even when the DSBs do not occur in the **normal** way. For the proposed model, these

findings could suggest that relatively **normal** interhomolog structural bridges may form even when the DSB occurs randomly in the genome rather than the...

...nucleated by crossover-committed interactions between both homologs and homeologs. Evidence from yeast suggests that DSBs occur **normally** in homeologous segments and that homology/homeology discrimination occurs later, but often prior to formation of permanent...During synaptic adjustment, the situation would be analogous to that in allohexaploid wheat except that nascent, otherwise **normal** , crossover-committed interactions within the destabilized chromosomal rearrangement region would be destabilized and released from their specific...

...e.g. 467, 468). Perhaps this is an additional effect of the stress transition, one that is **normally** counteracted by the presence of SC, in correlation with a tendency for SCs to be shorter at...

...axes, as in Psilotum (13) (Figure 20B-bottom). Furthermore, in the above model, such nonhomologous capture would **normally** be specifically precluded by the fact that stable DSB-mediated capture of a homolog axis is dependent...

...level aberrant (as implied by hyperresection of DSBs) but, in addition, bridge formation is uncoupled from its **normal** requirement for homologous interactions at the DNA level. This could explain why the hop2 mutant defect is...

...nonhomologous synapsis (369). In other situations, nonhomologous SC would have to form via an override of the **normal** dependency on homologous DNA/DNA contacts and might thus be less extensive than in hop2. A pms2...

...g. in plants and Bombyx triploids), which can be quite efficient, SC formation might be independent of **normal** nucleation because the foldback point brings two AEs close enough together to nucleate SC formation in the ...
...any specific bridge.

It may also be relevant that, in many cases, nonhomologous synapsis appears later than **normal** synapsis would have, sometimes explicitly as a second phase. Perhaps there is a removal of restrictions to nonhomologous synapsis at later stages or, alternatively, the "force for two-by-two association" becomes stronger if **normal** synapsis has not occurred.

WHY ARE REARRANGEMENT HETEROZYGOSITIES LOCALLY INHIBITORY OF CROSSING OVER?

Inversion and translocation heterozygotes...

...leptotene/zygotene transition, an immediately preceding transition or, when SC formation has failed to occur at the **normal** time, after the early/mid-pachytene transition.

ACHIASMATE MEIOSIS

In achiasmate Bombyx female meiosis, crossing over at...

...similar case(s). Does SC formation occur in the absence of any of the molecules or machinery **normally** involved in DSB formation and ensuing events? Or are some components of recombination-related processes utilized, e...

...at diplotene (above) might be poised to evolve into achiasmate organisms, which retain SC even longer than **normal** , in substitution for,

or stabilization of, homology-dependent connections other than crossovers (above).

CHIASMA TERMINALIZATION
A classical...on adjacent TFs to form a ladder-like CE layer. The individual layers are connected by occasional **vertical** fibers linking pillars on top of each other and keeping the layers in approximate register. Directions of...32. Barlow AL, Hulten MA. 1998. Combined immunocytogenetic and molecular cytogenetic analysis of meiosis I oocytes from **normal** human females. Zygote 6:27-38
33. Barlow AL, Hulten MA. 1998. Crossing over analysis at pachytene...

...Cell 98:249-59
49. Bogdanov YuF. 1977. Formation of cytoplasmic synaptonemal-like polycomplexes at leptotene and **normal** synaptonemal complexes at zygotene in Ascaris suum male meiosis. Chromosoma 61:1-21
50. Bojko M. 1983...

33/3,K/19 (Item 2 from file: 98)
DIALOG(R)File 98:General Sci Abs/Full-Text
(c) 2002 The HW Wilson Co. All rts. reserv.

03774006 H.W. WILSON RECORD NUMBER: BGSI98024006
A search for an inexpensive calculational method for the reliable prediction of the first adiabatic and vertical ionization potentials of carbenes. Photoelectron spectra of two stable carbenes.
Muchall, Heidi M
Werstiuk, Nick H; Choudhury, Biswajit
Canadian Journal of Chemistry (Can J Chem) v. 76 no2 (Feb. '98) p. 221-7
SPECIAL FEATURES: bibl il ISSN: 0008-4042
LANGUAGE: English
COUNTRY OF PUBLICATION: Canada

ABSTRACT: Photoelectron (**PE**) spectra of two stable carbenes 7 and 8 have been recorded and the spectra have been interpreted...

...and Becke3PW91 methods (3-21G(*) and 6-31+G* basis sets) as well as the CBS-4 **model** . For the first **vertical** IP, the HAM/3, Becke3LYP, and Becke3PW91 methods have been employed. CBS-4 and DFT calculations show...

33/3,K/20 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext
(c) 2002 ProQuest. All rts. reserv.

04459716 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Evolution of moist-baroclinic normal modes in the nonlinear regime
Fantini, Maurizio
Journal of the Atmospheric Sciences (IJAT), v56 n17, p3161-3166, p.6
Sep 1, 1999
ISSN: 0022-4928 JOURNAL CODE: IJAT
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2268

TEXT:
... We will focus in this note on the early stages of evolution of the most unstable linear **normal modes** into the nonlinear regime, shortly after the nonlinear terms, marked by the coefficient y in the equations...

...that the meridional displacement of the perturbations obtained in F95 is not present in the primitive equation (**PE**) simulations, and that important aspects of the evolution are sensitive to the formulation of perturbation buoyancy, which...

33/3,K/21 (Item 2 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext
(c) 2002 ProQuest. All rts. reserv.

04069443 (USE FORMAT 7 OR 9 FOR FULLTEXT)
The Power of Apartheid: State, Power and Space in South African Cities
Bond, Patrick
Journal of Southern African Studies (JSAS), v24 n3, p592-594, p.3
Sep 1998
ISSN: 0305-7070 JOURNAL CODE: JSAS
DOCUMENT TYPE: Book Review-Favorable
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1409

TEXT:
... fades - and regrettably is not revisited in Robinson's brief, ambivalent conclusion - leaving her central chapters on **PE** 's development from 1923 to 1972 to illustrate themes very much of concern to anyone, coming from...

...what is happening, and it is here that readers would have welcomed attention to the durability of **normalizing** , **modernizing** , housing policy discourses notwithstanding their failure since 1994.
But because of its concreteness, The Power of Apartheid...

33/3,K/22 (Item 3 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext
(c) 2002 ProQuest. All rts. reserv.

04032272 (USE FORMAT 7 OR 9 FOR FULLTEXT)
A short echo 1H spectroscopy and volumetric MRI study of the corpus striatum in patients with obsessive-compulsive disorder and comparison subjects
Bartha, Robert; Stein, Murray B; Williamson, Peter C; Drost, Dick J; et al
American Journal of Psychiatry (GPSI), v155 n11, p1584-1591, p.8
Nov 1998
ISSN: 0002-953X JOURNAL CODE: GPSI
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5553

TEXT:
... footnote to figu' 2 contains a complete list of the metabolites and macromolecules included i' the spectrum **model** .' ' Metabolite levels were **normalized** to the unsuppressed water signal followin' correction for the partial volume effect (29, 35) of the ratio...disorder. Arch Gen Psychiatry 1995; 52:393-398' ' 14. Aylward EH, Harris GJ, Hoehn-Saric R, Barta **PE** , Machlin SR, Pearlson GD' Normal caudate nucleus in obsessive-compulsive disorder assessed by' quantitative neuroimaging. Arch Gen...

33/3,K/23 (Item 1 from file: 141)
DIALOG(R)File 141:Readers Guide

(c) 2002 The HW Wilson Co. All rts. reserv.

03536876 H.W. WILSON RECORD NUMBER: BRGA97036876 (USE FORMAT 7 FOR FULLTEXT)
Industry resources 1997/1998.
AUGMENTED TITLE: special issue
TCI (TCI) v. 31 (June/July '97) p. 14-18+
WORD COUNT: 215730

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... 5:00PM, EST
Develops Behaviours, a software based media control system. Behaviors includes data bases and 3D **models** for automated luminaires and runs under Windows NT with extensive use of graphics environment. Also offering design...

33/3,K/24 (Item 2 from file: 141)
DIALOG(R)File 141:Readers Guide
(c) 2002 The HW Wilson Co. All rts. reserv.

03008752 H.W. WILSON RECORD NUMBER: BRGA95008752 (USE FORMAT 7 FOR FULLTEXT)
The right connections.
AUGMENTED TITLE: high-speed fax modems
Angus, Jeff.
PC World v. 12 (Sept. 1994) p. 190-4+
WORD COUNT: 6732

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... have to be rebooted.
Either use an internal fax-modem or make sure your external model is **connected** through a **serial** port that uses a 16550 UART. About 50 percent of even the highspeed 486DX and Pentium systems...

...use the lower-end 8250 UART, which will almost certainly fall with a 28.8-kbps fax- **modem** working at its **normal** speed. You can buy a serial port that's equipped with a 16550.
To see which UARTs...

33/3,K/25 (Item 1 from file: 370)
DIALOG(R)File 370:Science
(c) 1999 AAAS. All rts. reserv.

00507477 (USE 9 FOR FULLTEXT)
Turbulent Transport Reduction by Zonal Flows: Massively Parallel Simulations
Lin, Z.; Hahm, T. S.; Lee, W. W.; Tang, W. M.; White, R. B.
Princeton Plasma Physics Laboratory, Princeton University, Post Office Box 451, Princeton, NJ 08543, USA.
Science Vol. 281 5384 pp. 1835
Publication Date: 9-18-1998 (980918) Publication Year: 1998
Document Type: Journal ISSN: 0036-8075
Language: English
Section Heading: Reports
Word Count: 2131

(THIS IS THE FULLTEXT)

Text: Turbulence shear suppression by E x B flows (plasma flows induced by an electric field **perpendicular** to a magnetic field line) is the most likely mechanism responsible for the transition to various forms ...

...was implemented as a platform-independent program and achieved nearly perfect scalability on various massively parallel processing (**MPP**) systems (for example, CRAY-T3E and Origin-2000 supercomputers). This scalability enables us to fully use the rapidly increasing **MPP** computer power that presently allows routine nonlinear simulations of more than 10.sup(8) particles to treat...is the ion temperature, and T.inf(e) is the electron temperature. The size of the plasma **column** was a = 160 (rho) .inf(i), where (rho) .inf(i) is the thermal ion gyroradius measured at... Figure Removed

Figure F3
Caption: Instantaneous radial profile of E x B shear **normalized** to gyrofrequency ((Omega) .inf(i)) in local (dotted) and global (solid) simulations with broad profile...

33/3,K/26 (Item 2 from file: 370)
DIALOG(R)File 370:Science
(c) 1999 AAAS. All rts. reserv.

00504174 (USE 9 FOR FULLTEXT)
Active Deformation of Asia: From Kinematics to Dynamics
England, Philip; Molnar, Peter
P. England, Department of Earth Sciences, Oxford University, Oxford OX1 3PR, UK. ; P. Molnar, Department of Earth, Atmospheric, and Planetary Sciences, Massachusetts Institute of Technology, Cambridge, MA 02139, USA.
Science Vol. 278 5338 pp. 647
Publication Date: 10-24-1997 (971024) Publication Year: 1997
Document Type: Journal ISSN: 0036-8075
Language: English
Section Heading: Reports
Word Count: 2781

(THIS IS THE FULLTEXT)

...Text: is not confined to narrow bands, but is spread over regions hundreds to thousands of kilometers in **horizontal** extent. The actively deforming part of Asia, which we consider here, is larger than several of the...
...stress nor strain can be measured at depth within the lithosphere, it is impossible to determine the **vertical** gradients of stress in Eq. 1 (B6) . We therefore treat deformation of the lithosphere in terms of **vertical** averages of stress and strain rate in a thin sheet of fluid [for example, (B3) (B4) (B7)]. This simplification is appropriate where the **horizontal** dimensions of a region of active deformation exceed by many times the thickness of the lithosphere (B8...

...km, density contrasts within the lithosphere are isostatically compensated. Thus, the weight per unit area of any **column** of rock is supported by the **vertical** traction, (final-sigma) .inf(zz), on its base (final-sigma) .inf(zz)(z) = -g Limit{ (integral) Low...

...The **horizontal** equations in Eq. 1 may be expressed in terms of deviatoric stress (B9) , and simplified by taking **vertical** averages and neglecting shear tractions on the base of the lithosphere [for example, (B10)] L ((partial-derivative sup(th) component of the deviatoric stress tensor, averaged **vertically** through the lithosphere, and (Gamma) = -Limit{ (integral) Low=0, Upper=L} (final-sigma) .inf(zz)(z)dz...

...0, Upper=L} Limit{ (integral) Low=0, Upper=z} (rho) (z (prime))dz (prime) For isostatically balanced **columns** of lithosphere, differences in (Gamma) are equal to differences in the gravitational potential energy per unit area between **columns** (B4) (B10) (B11) (B12...

...Equation 3 states that **horizontal** gradients of the deviatoric stress required to deform a thin viscous sheet are balanced by **horizontal** gradients of its gravitational potential energy (B4) (B7) (B10) (B11) . A simple test of the hypothesis that...

...a knowledge of the density structure of the lithosphere. Because there are no observations of components of **vertically** averaged stress in the lithosphere and no direct observations of the gravitational potential energy of the lithosphere...

...The stresses in Eq. 3 can be related to deformation by specifying a relation between the **vertically** averaged deviatoric stresses and the **vertically** averaged strain rates in the lithosphere. The **vertical** averages of a wide range of possible rheological profiles for the continental lithosphere probably obey a relation...

...Gamma) * = (Gamma) /BL x (1 sec).sup(1/).sup(n) is the dimensionless potential energy of a **column** of lithosphere...
...mantle, the difference (Delta) (Gamma) in gravitational potential energy per unit area between any two isostatically balanced **columns** of lithosphere is simply (Delta) (Gamma) = (g (rho) .inf(c)/2)[1 -((rho) .inf(c)/ (rho) .inf...

...mantle, and S.inf(1) and S.inf(2) are the thicknesses of crust in the two **columns** . We use Eq. 10 to approximate gravitational potential-energy differences, estimating crustal thickness from surface elevation by assuming isostatic balance with a standard **column** of oceanic ridge (B14) . We recognize that possible variations in the thickness and temperature structure of the...strain-rate components within each triangle to the relative velocities of its vertices, forming a set of **normal** equations that could be solved to yield the velocity field (Fig. 1). Self-consistent strain rate components...figure 9 of (B19)], converted to dimensionless stress using Eq. 7, with n = 3. Bars show principal **horizontal** stresses; black bars correspond to contractional stress and white bars to extensional stress. Lengths of symbols are...

...Figure Removed

Figure F4
Caption: Calculated dimensionless potential energy (**PE**) (contours in Fig. 3) against the potential energy calculated from Eq. 10, using observed values of surface...

...around Lake Baikal. Open symbols are for the remainder of the region shown in Fig. 3. The **straight line** has a slope of 1.3 x 10.sup(12) N m.sup(-2) s.sup(1...

...Figure Removed

Begin Table : **Columns** 1 - 3 of 4

Caption:
Strain rate (|$$ (over-dot) epsilon = equals even dots/<RAD><RCD>2
</RCD...

33/3,K/27 (Item 3 from file: 370)
DIALOG(R)File 370:Science
(c) 1999 AAAS. All rts. reserv.

00500434 (USE 9 FOR FULLTEXT)
Structural Analysis of Substrate Binding by the Molecular Chaperone DnaK
Zhu, Xiaotian; Zhao, Xun; Burkholder, William F.; Gragerov, Alexander; Ogata, Craig M.; Gottesman, Max E.; Hendrickson, Wayne A.
X. Zhu, X. Zhao, W. F. Burkholder, A. Gragerov, M. E. Gottesman, and W. A. Hendrickson are in the Department of Biochemistry and Molecular Biophysics, College of Physicians and Surgeons, Columbia University, New York, NY 10032, USA. X. Zhu and W. A. Hendrickson are also with the Howard Hughes Medical Institute, Columbia University. W. F. Burkholder and M. E. Gottesman are also in the Institute of Cancer Research, Columbia University, New York, NY 10032, USA. C. M. Ogata is with the Howard Hughes Medical Institute, National Synchrotron Light Source, Brookhaven National Laboratory, Stony Brook, New York, USA.
Science Vol. 272 5268 pp. 1606
Publication Date: 6-14-1996 (960614) Publication Year: 1996
Document Type: Journal ISSN: 0036-8075
Language: English
Section Heading: Research Articles
Word Count: 7753

(THIS IS THE FULLTEXT)
...Text: They are named for their selective expression in response to metabolic stress, but they are also expressed **normally** and participate in various cellular processes, including the folding of nascent polypeptides, assembly and disassembly of multimeric...of helix aB, and the shortest dimension coincides with the direction of the peptide extension and is **perpendicular** to the plane of Fig. 2, A and B. This flattened profile (Fig. 2, B and C...

...beta) 6, (beta) 7, (beta) 8) is a rather regular, twisted (beta) sheet with hairpin (beta) turns **connecting** the **successive** strands, whereas the top sheet ((beta) 5, (beta) 4, (beta) 1, (beta) 2) is highly irregular (top...defining (beta) bulges in (beta) 2 and (beta) 5, which in turn project the loops out almost **perpendicular** to the top (beta) sheet. There are three crossover connections between the sheets. Two of these form ... Begin Table : **Columns** 1 - 4 of 9

Caption:
Statistics for MAD data and phase determination from a selenomethionyl crystal. The...

33/3,K/28 (Item 4 from file: 370)
DIALOG(R)File 370:Science
(c) 1999 AAAS. All rts. reserv.

00500374 (USE 9 FOR FULLTEXT)
The Whole Structure of the 13-Subunit Oxidized Cytochrome c Oxidase at 2.8

angstrom

Tsukihara, Tomitake; Aoyama, Hiroshi; Yamashita, Eiki; Tomizaki, Takashi; Yamaguchi, Hiroshi; Shinzawa-Itoh, Kyoko; Nakashima, Ryosuke; Yaono, Rieko; Yoshikawa, Shinya
T. Tsukihara, H. Aoyama, E. Yamashita, T. Tomizaki, H. Yamaguchi are at the Institute for Protein Research, Osaka University, 3-2 Yamada-oka, Suita 565, Japan. ; K. Shinzawa-Itoh, R. Nakashima, R. Yaono, S. Yoshikawa are at the Department of Life Science, Himeji Institute of Technology, Kamigohri Akoh, Hyogo 678-12, Japan.
Science Vol. 272 5265 pp. 1136
Publication Date: 5-24-1996 (960524) Publication Year: 1996
Document Type: Journal ISSN: 0036-8075
Language: English
Section Heading: Research Articles
Word Count: 7797

(THIS IS THE FULLTEXT)

...Text: 12 transmembrane helices, without any large extramembrane part (Fig. 3A). This subunit is cylindrical and is oriented **perpendicularly** to the membrane surface. Three semicircular arrangements of transmembrane helices, each composed of four helices, form a...

...the top). Two of the three semicircles hold hemes a and a.inf(3), respectively, which are **perpendicular** to the membrane plane. The twisted hydroxyl ...are fully consistent with those of bacterial enzyme (B7) . The helices of subunit I are not completely **perpendicular** to the membrane surface plane, but one end of each helix is placed on the top left and the other end on the bottom right (angles of 20.Deg. to 35.Deg. against the **vertical** line from the membrane plane) when the cytosolic surface of subunit I is "up". The extramembrane portion...As stated above, most of the transmembrane helices are not **vertical** to the membrane plane and usually are not parallel to each other. Any one of a pair...form a triangle, the plane of which is essentially parallel to the shortest hydrogen-bond system and **perpendicular** to ...Phospholipids. Eight phospholipids, five phosphatidyl ethanolamines (**PE**) and three phosphatidyl glycerols (PG), have been clearly demonstrated in the multiple isomorphous replacement electron density distribution...

...transmembrane region as would be expected if these phospholipids are in the lipid bilayer (Fig. 7). One **PE** and one PG are placed on the cytosolic side and the other six, on the matrix side...

...the transmembrane surface of subunit I on the opposite side from the subunit III contact and one **PE** on subunit VIa (Fig. 7...Trp.sup(99) of the same subunit (Fig. 9A). The sterol group of the cholate is located **horizontally** in the membrane surface plane on the cytosolic side. An OH group at position 12 of the...

...forms a hydrogen bond to the oxygen atom of the phosphoester of PE5. The sterol group is **vertical** , with the acid terminal on the bottom, in line with the phospholipids on the matrix side (Fig...Figure Removed

Begin Table : **Columns** 1 - 3 of 3

Caption:
Geometries of interaction between two adjacent transmembrane a helices.

Inclination degree Orientation...

33/3,K/29 (Item 1 from file: 553)
DIALOG(R)File 553:Wilson Bus. Abs. FullText
(c) 2002 The HW Wilson Co. All rts. reserv.

04044591 H.W. WILSON RECORD NUMBER: BWBA99044591 (USE FORMAT 7 FOR FULLTEXT)
Explaining movements in UK stock prices.
Cuthbertson, Keith
Hayes, Simon; Nitzsche, Dirk
Quarterly Review of Economics and Finance v. 39 no1 (Spring 1999) p. 1-19
LANGUAGE: English
WORD COUNT: 7287

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... the dividend-price ratio in the VAR (row 1, Table 3). The persistence measure for excess returns **Pe** is 1.55 (s.e. = 0.59) and the proportionate contribution of news about future excess returns...

...capital gains and losses. This result is therefore broadly consistent with that found for the real returns **model** .

The results in **row** 2 of Table 3 show that variations in the variables in the VAR do not appreciably affect...

33/3,K/30 (Item 2 from file: 553)
DIALOG(R)File 553:Wilson Bus. Abs. FullText
(c) 2002 The HW Wilson Co. All rts. reserv.

03064451 H.W. WILSON RECORD NUMBER: BWBA95064451 (USE FORMAT 7 FOR FULLTEXT)
Editor & Publisher 1995 syndicate directory: 70th annual directory of syndicated services.
Editor & Publisher, the Fourth Estate (Ed Publ Fourth Estate) v. 128 sec2 (July 29 '95) p. 28S-178S
LANGUAGE: English
WORD COUNT: 127439

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... SHN
Rosenfeld, Stephen -- Stephen S. Rosenfeld LAT-WP
Rosenkrantz, Linda -- Contemporary Collectibles CNS
Rosenthal, A.M. -- Rosenthal **Column** (New York Times news Services) NYT
Rosenthal, Harry -- Over Fifty APN
Rosenthal, Neil -- Intimacy DAA
Ross, Alicia...Zaslow, Jeffrey -- All That Zazz CATF
Zebora, Jim -- What's Brewing WB
Zisman, Lawrence H. -- Marketing Maven **MPP**
Zisman, Lawrence H. -- Marketing Yourself **MPP**
Zollman, Joseph -- Judaica Stamp & Coin Reporter STA
Zollman, Joseph -- Learning Through Stamps STA
Zollman, Joseph -- Spotlight on...ing/fax/mail -Patricia Arrigoni ATS
Marketing Maven -- 1tw -600 -man/mail -Lawrence H.

Zisman/Anabel Kligerman **MPP**
Marketing Yourself -- 2tw -600 -man/mail -Lawrence H.
Zisman/Anabel Kligerman **MPP**
Matters of the Heart -- 1tw -600 -orp/mail/DF/ctc/disk -Dr.
Marshall Franklin CNS
*McGee's...disk/rom/line/fax -Staff NAPS
Marketing Maven -- 1tw -600 -man/mail -Lawrence H.
Zisman/Anabel Kligerman **MPP**
Media -- 1tw -hpt -orp/mail AMW
* Mexican Stock Market -- 5tw -200-300 -wire/DNS -Various
UPI

Meyers...